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NEW PLATFORMS FOR ELECTRONIC DEVICES: N-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS, COMPLEMENTARY CIRCUITS, AND NANOWIRE TRANSISTORS

Committee:

Ananth Dodabalapur, Supervisor

Jack Lee

Ray Chen

Dean P. Neikirk

Yueh Lin Loo

NEW PLATFORMS FOR ELECTRONIC DEVICES: N-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS, COMPLEMENTARY CIRCUITS, AND NANOWIRE TRANSISTORS

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Byungwook Yoo, B.S.; M.S.

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Dedication

To my mother, Soon Hee Kim, and the memory of my father, Myung Shik Yoo

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NEW PLATFORMS FOR ELECTRONIC DEVICES: N-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS, COMPLEMENTARY CIRCUITS, AND NANOWIRE TRANSISTORS

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This work focused on the fabrication and electrical characterization of electronic devices and the applications include the n-channel organic field-effect transistors (OFETs), organic complementary circuits, and the germanium nanowire transistors. In organic devices, carbonyl-functionalized α,ω-diperfluorohexyl quaterthiophenes (DFHCO-4T) and N,N' –bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2) are used as n-type semiconductors. The effect of dielectric/electrode surface treatment on the response of bottom-contact devices was also examined to maximize the device performance. Some of innovative techniques that employ the conducting polymer, poly(3,4-ethylenedioxythiophene) / poly(styrene sulfonate) (PEDOT/PSS) for the fabrication of OFETs, were compared and investigated. The device performance and the fabrication yield were also considered. Organic complementary ring oscillators and D flip-flops were demonstrated with PDI-8CN_2 and pentacene as the n-type and p-type material, respectively. Both circuits recorded the highest speed that any organic

transistor-based complementary circuit has achieved to date. The speed of these complementary circuits will be enhanced by increasing the mobility of n-channel further as well as reducing channel lengths and overlap capacitances between the source/drain electrodes and the gate. The semiconductors should be solution processible to be compatible with the inexpensive fabrication techniques envisioned for printed electronic circuits. PDI-8CN_2 was used for solution-processed n-channel OFETs and the various parameters are compared for the optimization of devices. Utilizing optimized process parameters and surface treatments for solution-deposited PDI-8CN_2 OFETs, we have successfully shown the first fabrication of complementary organic ring oscillators and D-flip flops by the micro-injection of the solution of both p-type and n-type materials in air. One of the potential platforms for low cost fabrication on flexible substrates is the use of inorganic semiconductor nanowires. Accordingly, the germanium nanowire FETs were fabricated and characterized. Conductivity enhanced PEDOT/PSS was employed as the electrode material for nanowire transistors to improve the electrical contacts to the source and drain.

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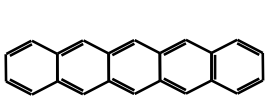
CHAPTER 1 INTRODUCTION

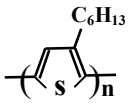
1.1 Organic materials

1.1.1 ORGANIC SEMICONDUCTORS

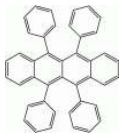
From an electrical point of view, polymers have been considered as insulators. However, since the landmark discovery of the metallic properties of polyacetylene in 1977 [1,2], pi-conjugated polymers and small organic molecules have been investigated for their semiconducting properties. Organic semiconductors are bonded by weak Van der Waals forces in contrast to inorganic materials that are constituted by covalent or ionic bonds. Therefore, synthesis of organic semiconductors can be carried out at the molecular level and suitable selections of structural units need to be made to achieve the required thermal, structural, charge transport and electrochemical properties. Most organic semiconductors are ambipolar; however, the existence of traps causes them to preferentially transport either electrons or holes in field-effect transistors (FETs). For simplicity, henceforth, materials forming n-channel FETs are referred to as n-type semiconductors and those forming p-channel FETs are referred to as p-type semiconductors The nature of the charge carrier transport can be approximately decided based on the selection of electron-deficient moieties (n-channel FETs) or electron-rich moieties (p-channel FETs) in the molecular structure of these materials.



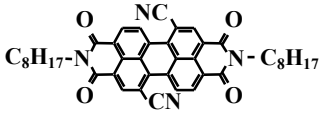
Pentacene



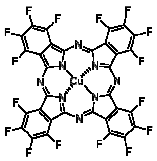
P3HT



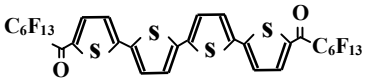
Rubrene



PDI-8CN_2



FCuPc



DFHCO-4T

Fig. 1.1 Examples of p-type and n-type organic semiconductors

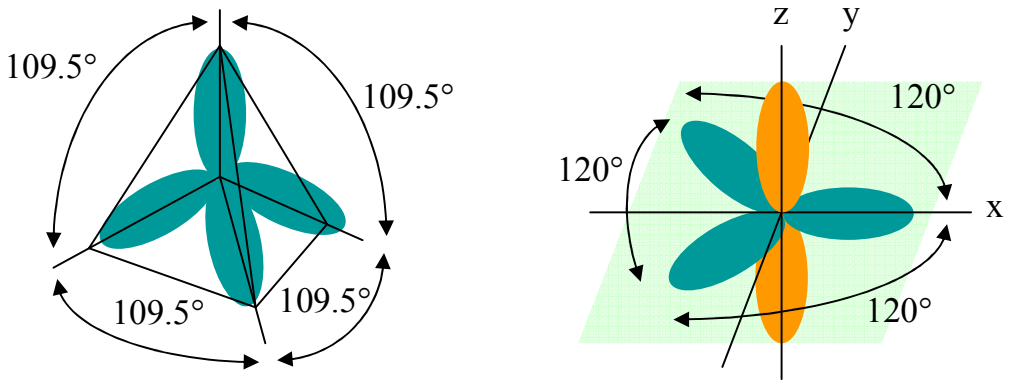
A number of high performance p-type and n-type organic semiconductors are shown in Fig. 1.1. Due to the challenges of synthesizing stable and high performance n-type organic semiconductors, most research has been oriented towards devices with p-type semiconductors such as pentacene, regioregular poly(3-hexylthiophene) (P3HT), and rubrene. N-type semiconductors are necessary in applications such as organic light emitting diodes and complementary metal oxide semiconductor (CMOS) circuits. N,N'-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2), copper hexadecafluorophthalocyanine (F_{16}CuPc), and carbonyl functionalized (α,ω-diperfluorohexyl-4T) (DFHCO-4T) are examples of n-type organic semiconductors.

1.1.2 TRANSPORT IN ORGANIC SEMICONDUCTORS

The main difference between inorganic and organic semiconductors is the nature of charge transport. In the inorganic crystalline semiconductors, carrier transport takes place in well-defined bands. In this case, charge carriers have a high mobility (~ 10^3 cm^2/Vs) at room temperature and the mobility is limited by lattice vibrations (phonons) which scatter the carrier. Therefore, the mobility decreases as the temperature increases. Electron transfer between oligomers and polymers is less facile than transfer between covalently bonded atoms due to the weaker interaction between the molecules in organic semiconductors and the stronger interaction of carriers with phonons. Band transport is found in crystalline organic semiconductors at low temperature. The energy states are localized in disordered organic semiconductors and carrier transport takes place by hopping. The charge carrier jumps from one chain to another to contribute to the transport and this gives rise to low carrier mobility in hopping transport. Hopping is assisted by phonons and the mobility increases with temperature [3,4]. An intermediate stage is found in partially ordered, polycrystalline organic semiconductors. The material is highly ordered within the grains. However, the presence of grain boundaries limits the mobility, because the disorder at grain boundaries leads to some localized states within the energy gap which trap the mobile charge carriers. In some cases, intra-grain transport exhibit features of band-like transport.

Multiple trapping and release (MTR) model is used to explain charge transport in organic semiconductors [5]. According to this model, there are distributions of traps in the forbidden energy gap above the valence band edge.

At low gate voltage, most of the charge carriers injected in the semiconductor are trapped into these localized states. The deepest traps are filled first and the carriers can be thermally released. As the gate voltage increases, more traps are filled and the Fermi level approaches the valence band edge. At a sufficiently high voltage, all trap states could be filled and the subsequently injected carriers move with the mobility associated with carriers in the valence band [6,7]. However, this model does not completely account for the temperature independent mobility which has been reported in some cases such as pentacene and oligothiophenes [8-10]. Charge transport mechanisms between molecules could be band-like transport, hopping, or tunneling [11-14]. At room temperature, band transport requires that the moblility, $\mu \geq 1$ cm^2/Vs. If $\mu < 1$ cm^2/Vs, the nature/type of transport is hopping [9,15].



Four sp^3 hybrid orbitals

Three sp^2 orbitals and p_z orbital

Fig. 1.2 Different hybridization of carbon atoms

Polymers are formed of long chains of monomers which are repeated linking units held together by carbon bonds. A carbon atom bonds to the

surrounding atoms and is composed of either tetrahedral-symmetric covalent bonds (sp^3 hybridization) or hexagonal-symmetric covalent bonds (sp^2 hybridization). The hybridization of carbon atoms is illustrated in Fig. 1.2. When the carbon atoms undergo sp^3 hybridization, all of the four valence electrons equally participate in four sigma (σ) bonds with neighboring atoms; therefore the monomer chain is saturated in three-dimensional space which leads to a uniform bond angle of 109.5° and there is no free electron to contribute to electrical conduction [16]. The resulting structure results in an insulating polymer such as polyethylene. Polyethylene is formed by saturated sp^3 hybridized σ bonds. The resulting covalent bonds are strong and the electronic excitations from the bonding orbital to the anti-bonding orbital require a large amount of energy. Therefore, the energy gap is large and it gives rise to the characteristics of an insulating polymer.

On the other hand, a conjugated polymer such as polyacetylene is formed by sp^2 and p_z hybridization. As a result, one electron from s orbital and two electrons from p orbitals (p_x, p_y) hybridize to form a sp^2 orbital and three σ bonds are equally saturated in two-dimensional space leading to a uniform bond angle of 120° [16]. The fourth valence electron occupies the p_z orbital and forms the π bond, which is perpendicular to the plane of sp^2 orbital. This π electron is delocalized and the alternation in single and double bonds (conjugated bond) results in the semiconducting properties of organic molecules and polymers. The carbon atoms are linked by single bond when the chain is undimerized. [17]. A π bond is formed between every other pairs of nearest carbon atoms so that single bonds (σ bond) and double bonds (σ and π bonds) alternate along the entire chain. When this state of the chemically doped

polymer chain is excited by thermal activation, a free radical and cation are coupled through the lattice distortion and a polymer chain will form a polaron which is a charge accompanied by the deformation of the lattice. In organic crystals composed of small molecules, the charge carriers coupled to lattice distortions. The classification of properties of organic and inorganic semiconductors is summarized in Table 1.1.

Semiconductors	Organic		Inorganic crystalline
	Disordered	Crystalline	
Bond type	Van der waals		Covalent
Charge carrier	Polaron		Electron or hole
Moblility	Low	Medium	High
Thermal behavior	Thermally activated	Thermally activated / limited	Thermally limited

Table 1.1 Summary of the differences in properties between organic and inorganic semiconductors

1.2 Organic devices

1.2.1 ORGANIC FIELD-EFFECT TRANSISTORS

Since the first demonstration of organic field-effect transistors (OFETs) with polyacetylene in 1983 [18], OFETs have attracted considerable attention for use in a wide range of inexpensive and high volume applications such as radio-frequency identification tags, display drivers, smart cards, sensor arrays, electronic paper and photodetectors [19-26]. Many studies have been reported in recent years focusing on the fabrication of submicron OFETs, synthesis of new n-type thiophene derivatives, replacement of inorganic insulating layers, plastic transistors in active-matrix displays, electrode contacts by polymers, nanoscale ambipolar transistors and the fabrication of submicron OFETs by nanoimprint lithography [22,27-32]. As new materials which show improved performance (such as mobility, solution processibility) are synthesized, the range of applications for OFETs gets broader and low-cost applications can be achieved by use of solution-based processes. In order to commercialize the OFETs for application such as display drivers, the electrical properties should be comparable to or exceed the properties of the competing materials such as amorphous silicon (~ 1 cm^2/Vs). The most important parameters are the charge carrier mobility and the current on/off ratio.

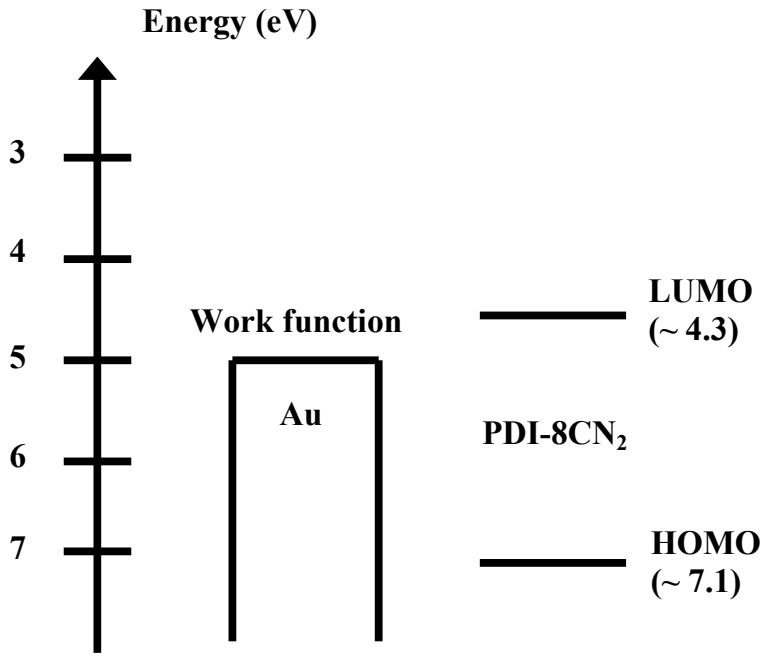


Fig. 1.3 The energy levels of gold and *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2)

The geometry of the organic thin-film transistor (OTFT) differs from the conventional silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET). The conducting channel usually formed with an accumulation layer in an OTFT. The Fermi level of gold and LUMO/HOMO levels of *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2) are shown in Fig. 1.3. When a negative voltage is applied to the gate, positive charges are induced at the source electrode. The Fermi level of gold is far from the HOMO level with respect to the LUMO level, making hole injection unfavorable. Even if holes are injected from the contact to the semiconductor, a high density of traps, that efficiently compete for the carriers prevent the formation of a mobile hole accumulation layer. Therefore, almost no current can pass through the

semiconductor layer, and the tiny value of the measured current essentially arises from leakage through the insulating layer. When the gate voltage is reversed, electrons can be injected from the source to the semiconductor. Accordingly, a conducting channel forms at the interface between insulator and semiconductor, and the charge can flow from source to drain by application of a drain voltage. As a result, PDI-8CN_2 is said to be a n-type semiconductor or a n-channel FET forming material.

There are two typical structures for an OTFT, namely the top contact structure and the bottom contact structure. The performance of the two configurations is generally different in OTFTs. In the top contact structure shown in Fig. 1.4 (a), the organic semiconductor is deposited on top of the gate dielectric layer. Source and drain electrodes are then patterned on top of the organic semiconductor layer by shadow masking. In the bottom contact structure shown in Fig. 1.4 (b), the source and drain electrodes are first defined prior to organic semiconductor deposition. Most reports on n-channel organic transistors use the top-contact structure [33-36]. The channel lengths created using shadow masking are typically large (> 25 μm) and unsuitable for fabricating fast circuits. In order to achieve the performance required for practical electronics, shorter channel lengths (< 10 μm) are required.

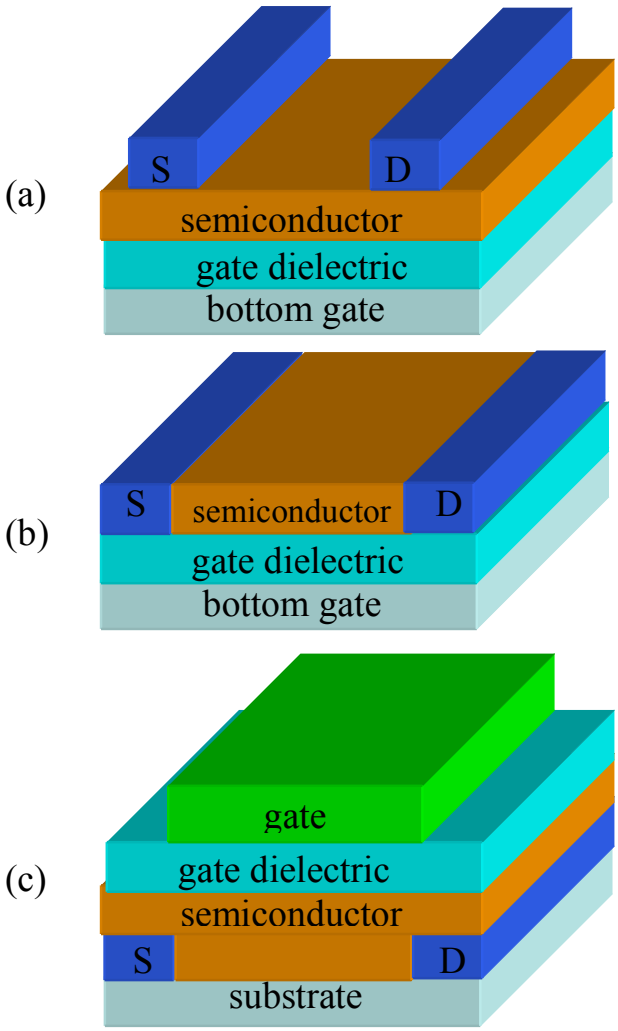


Fig. 1.4 Schematic representation of OTFT structure; (a) top-contact configuration (b) bottom-contact configuration (c) top gate configuration

In practical circuit fabrication, a bottom contact structure is more favorable as compared to a top contact structure, since conventional lithography can be more easily applied to bottom contact configurations without exposing the active organic material to solvents and chemicals. However, there are electronic

and morphological problems at the metal-to-semiconductor contact in the bottom contact structure. Metal electrodes can affect the growth of organic semiconductor films near the contact edges due to surface energy differences. Therefore, organic molecules are usually not well ordered near the contact electrodes and this area degrades the performance of the transistor. The influence of the contact becomes considerable as the channel length of an OTFT becomes smaller and most studies of bottom contact n-channel OTFTs employ large channel length devices ($\geq$ 50 μm) in which problems associated with contact injection are reduced [37-38].

There are two solutions for minimizing interface problems in the bottom contact configuration devices. One is the use of a conducting polymer such as poly(3,4-ethylenedioxythiophene)/poly(styrene sulfonate) (PEDOT/PSS) and the other is utilization of suitable self-assembled monolayers (SAM). The use of self-assembled monolayers (SAM) at the interface between the metal/insulator and the metal/semiconductor results in improved properties by lowering surface energy differences which assist the formation of ordered thin films [39-41]. The most common agent for passivating hydrophilic inorganic substrates is hexamethyldisilazane (HMDS), which coats the SiO_2 surface with a lower surface energy trimethylsilyl monolayer. Other silane functional groups such as octadecyltrichlorosilane (OTS), octyltrichlorosilane (OTS-8), and phenethyltrichlorosilane are also used for dielectric treatment. In order to coat metal electrodes, thiol-based SAM agents such as nitrobenzenethiol (NBT) and octadecanethiol (ODT) have been employed for modifying the surface energy of gold source and drain electrodes to facilitate charge carrier injection [42-44].

Depending on the method of fabrication, the gate electrode may be defined last so that the transistor structure is not inverted as shown Fig. 1.5 (c). In this configuration, the metal electrodes do not directly access the dielectric interface at which the field induced charge carriers are accumulated. These charge carriers are injected vertically from an electrode to the accumulation layer, move along the interface, and are collected at the drain electrode. A major advantage of this structure is that the semiconducting layer is inherently passivated by the gate dielectric. However, the insulating material and semiconductor should not be chemically reactive with each other.

Semiconductor deposition to form thin films can be done using vacuum deposition or solution deposition. Vacuum deposited semiconducting layers have good molecular ordering and thin films of oligomers or small molecules are deposited using this technique. However, the cost of fabrication is higher due to the necessary equipment required for vacuum deposition of thin films. Solution deposition by spin coating, ink-jet printing, or stamping is generally used for polymers and some soluble small molecules. It is a cost effective alternative to vacuum deposition. This technique holds promise for low cost, large area applications and mass production of organic devices. However, the crystalline order of the semiconducting layers is generally inferior with respect to vacuum deposited films.

A Typical plot of drain current (I_D) versus drain voltage (V_{DS}) at various gate voltage (V_G) is shown in Fig. 1.5(a). For a low drain-source voltage, the field created by the gate is uniformly distributed along the channel, giving rise to a uniform distribution of charge carriers. Therefore, the drain current is linearly proportional to the applied drain voltage (linear regime). In general, when

$0<|V_{DS}|<|V_G-V_T|$, the drain-source current is approximately determined by the standard MOSFET equation [45];

$$I_D = \frac{W\mu C_{ox}}{2L} \times \{2(V_G - V_T)V_{DS} - V_{DS}^2\}$$

where W is the channel width, L is the channel length, C_{OX} is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and μ is the field-effect mobility. In the linear regime, the mobility is calculated from the transconductance.

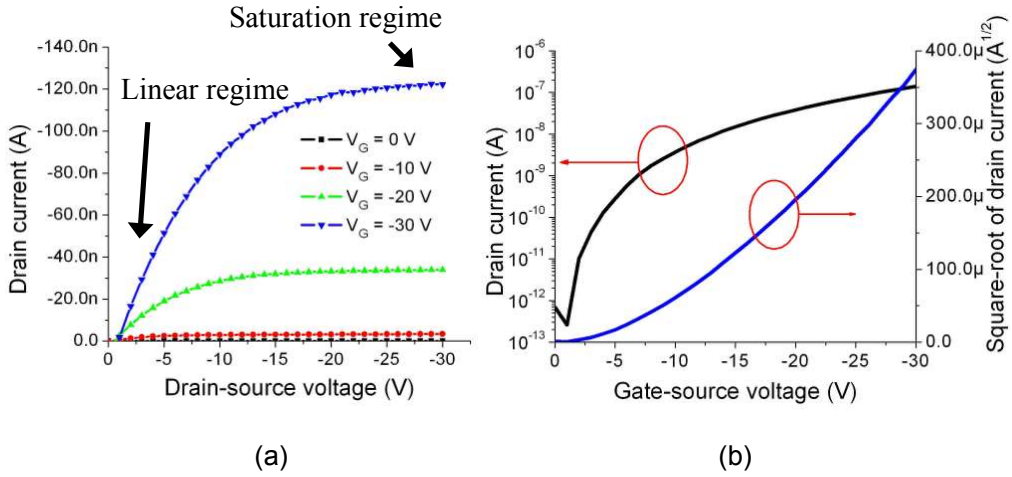


Fig. 1.5 Typical (a) output and (b) transfer characteristics of a pentacene OFET

When $|V_{DS}|$ is larger than $|V_G-V_T|$, the electric field created by the gate voltage at the drain contact becomes zero. In this saturation regime, additional drain voltage does not induce an increase in the drain current and the drain current is given by;

$$I_D = \frac{W\mu C_{ox}}{2L} \times (V_G - V_T)^2$$

In the saturation regime, the mobility is calculated from the slope of the plot of $|I_D|^{1/2}$ versus V_G as shown in Fig. 1.5(b).

The transport properties of OFETs are determined not only by the crystal structure of the organic semiconductor thin-films but also by the morphology of gate dielectrics. The electrode/semiconductor interface property determines the injection barrier and the dielectric/semiconductor interface property affects the molecular ordering within one or two monolayers of the organic semiconductor, as well the interface traps which also play a role in determining device mobility and subthreshold characteristics. The effective mobility in polycrystalline materials can be also affected by many factors such as trapping at a grain boundary, as well as intra-grain mobility. Therefore, better performance of OFETs can be achieved with smoother surfaces.

1.2.2 ORGANIC COMPLEMENTARY CIRCUITS

OFETs are attractive for their low processing cost compared to silicon and their compatibility with flexible substrates. P-channel OFETs fabricated from small molecules such as pentacene with mobilities more than 1 cm^2/Vs have been reported [44,46]. Even though this mobility is significantly lower than silicon, the performance of OFET is quite usable in a wide variety of circuit applications if implemented in an organic CMOS configuration.

In CMOS, p-channel and n-channel transistors operate in tandem to produce organic semiconductor circuit systems with low static power dissipation and high noise margins. Given comparable mobilities of constituent materials, a

CMOS system can operate faster than the equivalent p-channel circuit. The problem with this vision is that only a limited number of n-channel materials have been discovered so far. Most aromatic compound cores that exhibit semiconducting properties are generally better in transporting holes as compared to transporting electrons. The n-channel semiconductors that have been discovered have relatively low mobility, and tend to degrade quickly in atmosphere. In spite of these difficulties, there have been promising reports on high performance n-channel organic transistors using some special synthetic techniques in recent years [34,35,47]. The promise of a stable and processible organic n-type semiconductor opens up the possibility of developing an organic CMOS process.

1.3 Nanowire field-effect transistors

In addition to organic electronics, chemically synthesized nanomaterials such as nanowires and nanotubes have also been proposed as one of the promising alternatives to act as building blocks for future electronics such as field-effect transistors, logic gates, memory components, light emitting diodes, photo detectors, chemical sensors and lasers [48-57]. Their low dimensionality and high aspect ratio gives rise to unique physical and mechanical properties. Recently, many research groups have synthesized and used various kinds of nanowires such as silicon, germanium, cadmium sulfide, indium arsenide, gallium nitride, zinc oxide, and zinc selenide [58-64]. These one dimensional (1D) nanowires have a potential to be incorporated in structures with a flexible substrates and methods employing inexpensive processing techniques. In the context of such technological expectations, the optimization of material and device processing is required. For example, the chemical and electronic stabilities of nanowire are critical for device applications. Ease of mechanical manipulation and dispersibility in a variety of solvents is also important for their implementation.

CHAPTER 2 N-CHANNEL ORGANIC TRANSISTORS

2.1 Introduction

Organic field effect transistors (OFETs) have attracted considerable attention for use in applications such as radio-frequency identification tags, display drivers, smart cards, and sensor arrays [19-21]. Combining p-channel and n-channel transistors enables the fabrication of complementary circuits which exhibit lower power dissipation and superior noise margins compared to simple p-channel FET circuits. Hence, the investigation and development of materials that can be used in n-channel organic transistors is crucial for the development of practical organic electronics. N-type organic semiconductors have to satisfy a number of stringent criteria to show good characteristics; i) the HOMO/LUMO energies of the individual molecules should be at levels where electrons can be injected at accessible applied voltages; ii) the crystal structure of the material should provide sufficient overlap of frontier orbitals to allow efficient charge migration between neighboring molecules; iii) the solid should be extremely pure because impurities can act as charge carrier traps [67].

There are several reasons why the performance of n-channel organic transistors has been inferior with respect to p-channel organic transistors. Firstly, most conjugated aromatic cores have relatively small electron affinities so that these materials tend to transfer holes better than electrons. In such materials, the induced electrons tends to occupy trap states where they are

relatively immobile. Secondly, the trapping of electrons in the presence of oxygen and moisture results in the degradation in the performance of n-channel organic semiconductors very easily. Some of the earliest reports of n-channel organic transistors used electron-deficient perylene- and naphthalene- based semiconductors with good electrical properties and ambient device stability with N-fluroralkyl functionlization as well [64,65]. As the understanding of charge transport in organic materials has been improving, materials from oligothiophene, fullerene, and rylene imide families having top-contact mobilities consistently in excess of 0.1 cm2/V-s have been reported [32-36,66]. The recent high field-effect mobility values of sublimed n-channel bottom contact transistors are summarized in Table 2.1.

In this chapter, newly synthesized high-performance n-type semiconductors and the fabrication procedures of OFETs fabricated with these materials will be discussed. We then report the electrical characteristics of n-channel OFETs. The results of contact effects with top-contact transistors and the effects of various surface treatments on the electrical characteristics of bottom-contact transistors will be also discussed.

Compound	Mobility (cm^2/Vs)	W / L (μ m)	Refs
N,N' –bis(n-octyl)-dicyanoperylene-3,4: 9,10-bis(dicarboximide) (PDI-8CN_2)	0.14	200 / 4	68
Fullerine (C60)	0.65	500 / 50	69
Fullerine (C70)	0.066	500 / 50	69
3',4'-dibutyl-5,5'-bis(dicyanomethylene)-5,5"-dihydro-2,2':5',2"-terthiophene (DCMT)	0.18	300-1000/ 50-100 (W/L >10)	70
N,N' –dioctyl-3,4,9,10-perylene tetracar boxylic diimide (PTCDI-C8H)	0.6	1000 / 95	36
Hexadecafluorocopperphthalocyanine (F_{16}CuPc)	0.02	100 / 7.5	71

Table 2.1 Literature summary of high mobility n-channel transistors by thermal evaporation of n-type semiconductors in the bottom contact configuration

2.2 N-type organic semiconductors

2.2.1 CARBONYL-FUNCTIONALIZED A,Ω-DIPERFLUOROHEXYL QUATERTHIOPHENES

Recent work by Dr. Facchetti *et al.* demonstrated that selective functionalization and replacement of oligothiophene moieties with perfluorinated substituents enables the increase of electron mobilities [67]. In addition, they introduced the synthesis of new carbonyl-functionalized quaterthiophenes to improve the performance [35]. The quaterthiophene core was chosen because it exhibited reproducible high mobilities. There are several reasons why the carbonyl functionalization was selected; i) it introduces one of the stronger electron-withdrawing functionalities; ii) it allows additional fuctionalization in contrast to other electron-withdrawing groups such as CN; iii) it can be readily incorporated into π-conjugated cores [35]. New carbonyl-functionalized α,ω-diperfluorohexyl quaterthiophenes (DFHCO-4T) were synthesized and the chemical structure of DFHCO-4T is shown in Fig. 2.1.

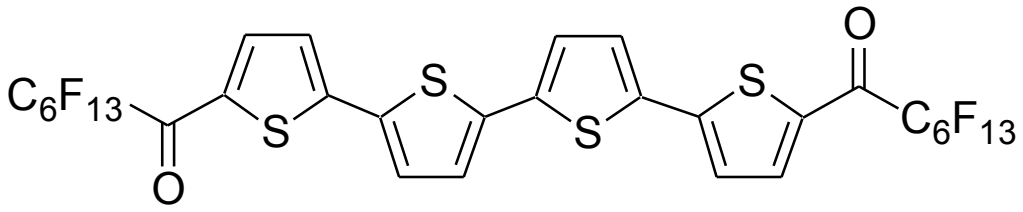


Fig. 2.1 The chemical structure of carbonyl-functionalized α,ω-diperfluorohexyl quaterthiophenes (DFHCO-4T)

2.2.2 N,N'-BIS(N-OCTYL)-DICYANOPERYLENE-3,4:9,10-BIS(DICARBOXIMIDE)

Perylene diimides (PDI) generally exhibit some detrimental properties such as; i) the material is not solution processable; ii) OFET performance degrades easily in air; iii) devices exhibit very large threshold voltages of ~75 V [33]. Therefore, many researchers have modified the PDI to ameliorate these problems by adding electron-withdrawing groups. For example, microwave conductivity measurements of 1,6,7,12-substituted PDI derivatives demonstrated that modulation of p–p overlap by twisting of the normally flat core can drastically affect carrier mobility [72]. As a result, these PDI based semiconductors have demonstrated great promise and hold the distinction of having one of the highest n-type mobility known of 0.6 cm^2/Vs uncorrected for contact resistance and 1.7 cm^2/Vs when corrected [32]. In addition to the outstanding electrical properties, PDI-based materials have demonstrated great promise due to their ability to yield semiconducting films from solution and air-stable device operation [33].

Among the n-type semiconductors investigated, one of the most promising PDI-based semiconductor candidates is *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2), which is a perylene derivative with the cyano group. This material is synthesized by Prof. Marks / Wasielewski groups at the Northwestern University. The cyano group increases solubility by decreasing molecular planarity and stabilizes charge carriers by lowering the energies of the lowest unoccupied molecular orbitals associated with electron transport [33]. Molecular structure of PDI-8CN_2 is shown in Fig. 2.2.

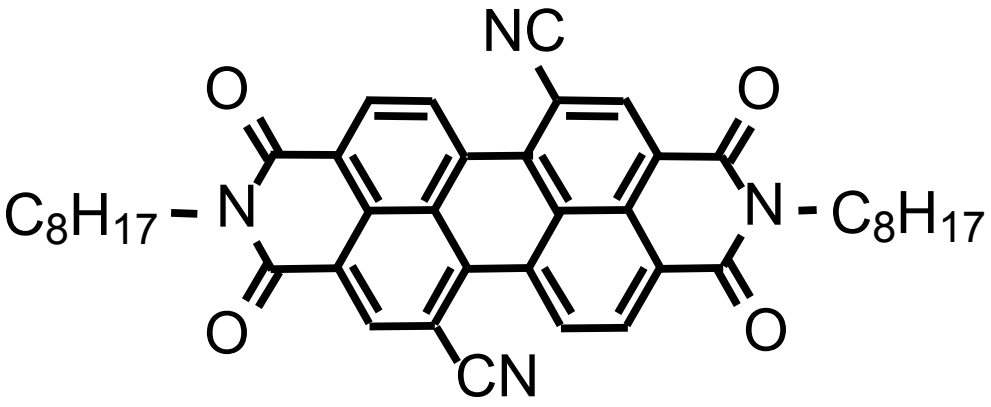


Fig. 2.2 The chemical structure of *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2)

2.3 Fabrication of n-channel field-effect transistors

2.3.1 TOP-CONTACT CONFIGURATION

Most reports on n-channel organic transistors use the top-contact geometry, in which the source and drain contacts are defined on top the semiconductor by shadow masking [32-35]. The channel lengths created using shadow masking are typically large (> 25 μm) and unsuitable for fabricating fast circuits. The fabrication process for top-contact devices is shown in Fig. 2.3. The substrates are heavily doped p-type silicon substrates serving as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric layer (34.5 nF/cm^2). SiO_2 is the most conventional gate dielectric in inorganic semiconductor FETs. It is also used in OFETs since it is chemically stable and the leakage current is very small. The substrates are cleaned by ultra-sonication in acetone, methanol, and deionized water. Oxygen plasma cleaning is then performed on the substrates (Fig. 2.3(a)). Prior to the semiconductor deposition, surface treatment of gate dielectric by hexamethyldisilazane (HMDS) is usually carried out to lower the surface energy. The semiconductor, DFHCO-4T, is thermally deposited on top of gate dielectric with a base vacuum of $\sim 5\times10^{-7}$ Torr and substrate temperature was increased to enhance the grain growth (Fig. 2.3(b)). The deposition rate of DFHCO-4T was 0.2-0.7 Å/s. The final fabrication step is deposition of gold (Au) electrodes on top of DFHCO-4T layer by e-beam evaporation with a shadow mask (Fig. 2.3(c)). Channel lengths and widths of devices were 1 mm and 10 mm, respectively. The devices were characterized by the Agilent 4155C semiconductor analyzer in a Desert Cryogenics vacuum probe

station at a pressure of ~ 1×10^{-3} Torr and the sample is held in darkness during the measurements.

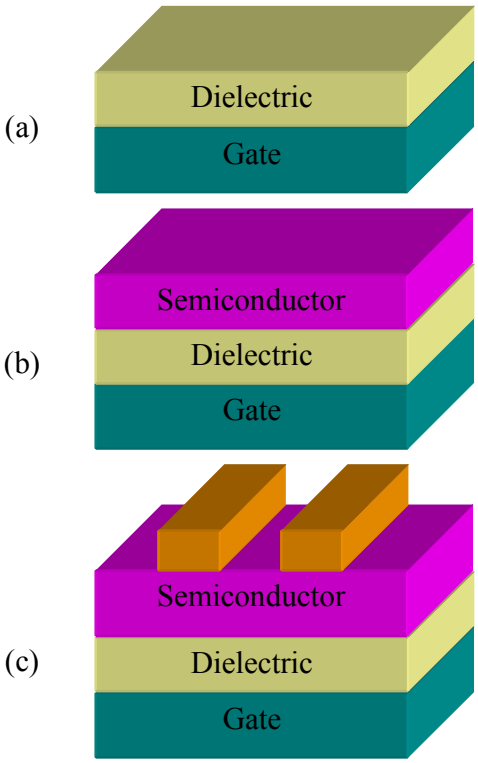


Fig. 2.3 The fabrication process of top-contact transistors; (a) dielectric surface cleaning (b) semiconductor deposition (c) metal electrodes deposition

2.3.2 ELECTRICAL CONTACTS

One of the important issues in the fabrication and operation of OFETs is the contact issue between the electrodes and the semiconductor layer. Matching the material properties of the electrodes to those of the organic semiconductors

will aid the improvement in device performance. It is not easy to decouple the contact characteristics and the organic film characteristics because the injection characteristics of the contact are not electrically constant as in a passive resistor. Several approaches have been investigated to characterize the contact resistance in OTFTs. Firstly, the surface potential of a device is measured with scanning Kelvin probe microscopy or AFM-based potentiometry, and the potential profile is measured along the entire channel [73,74]. However, the potential distribution of an OTFT is not really linear in the linear region [73]. Secondly, a four point probe measurement technique is employed to measure potentials of two points within a channel [75,76]. However, this method is not accurate for smaller contact resistances. The third approach uses the relationship of the total resistance with respect to different channel lengths [77,78]. The main limitations of this method are that all devices are required to have the same contact resistance with respect to the devices of different channel length. Due to the random arrangement of the organic semiconductors with respect to the electrodes, contact effects may not be consistent.

Recent work by Jung [79] *et al.* proposed a method to separate the channel resistance from the metal-to-semiconductor contact resistance in a bottom contact configuration of OTFT. Varying numbers of floating electrodes between the source and the drain electrodes are set, to change the number of contact interface in the channel and the effective channel lengths are kept constant. The channel resistance is extrapolated from the data and used to calculate the source/drain contact resistances. Although the effect of the contacts is not severe in top-contact configuration, the influence of the contact should be characterized in

detail in order to characterize the device completely. The contact characteristics of DFHCO-4T devices are measured accordingly in a top contact configuration.

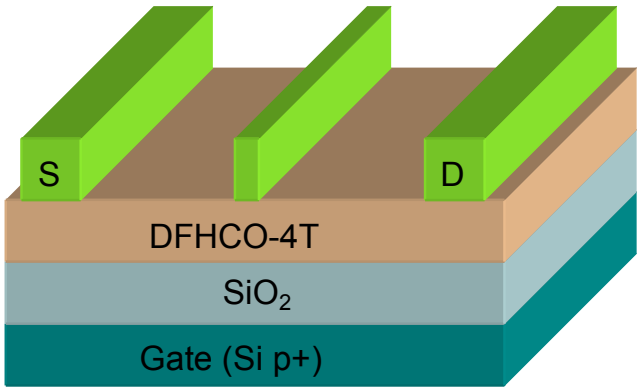


Fig. 2.4 Schematic of a device with one floating electrode; (S: source, D: drain). The effective channel length was kept constant regardless of the number of floating electrodes.

Fig. 2.4 shows the schematic of a device with one floating electrode. The width of these floating electrodes is the same as the channel width (W) of source/drain electrodes and the length of floating electrodes is 50 μm. The substrates were heavily doped p-type silicon substrates with 100 nm of thermally grown SiO_2. After wet cleaning and oxygen plasma cleaning of the substrates, DFHCO-4T was thermally deposited on top of the gate dielectric with the substrate temperature elevated to 60 ºC, at a vacuum of ~5×10^{-7} Torr. The deposition rate of DFHCO-4T was 0.2-0.7 Å/s. Gold electrodes and the floating electrodes were deposited on top of the DFHCO-4T layer by e-beam evaporation with a shadow mask. Effective channel lengths of devices were kept constant at 840 μm and the channel widths of devices were 10 mm.

2.3.3 BOTTOM-CONTACT CONFIGURATION

Semiconductors are usually deposited using a shadow mask in the top contact configuration to make the fabrication process easier. However, the use of the shadow mask technique is impractical and complicated if the scale of device dimensions is less than a few micrometers. Therefore, small channel length devices are fabricated with a bottom contact configuration and the fabrication process of bottom-contact PDI-8CN_2 devices is shown in Fig. 2.5.

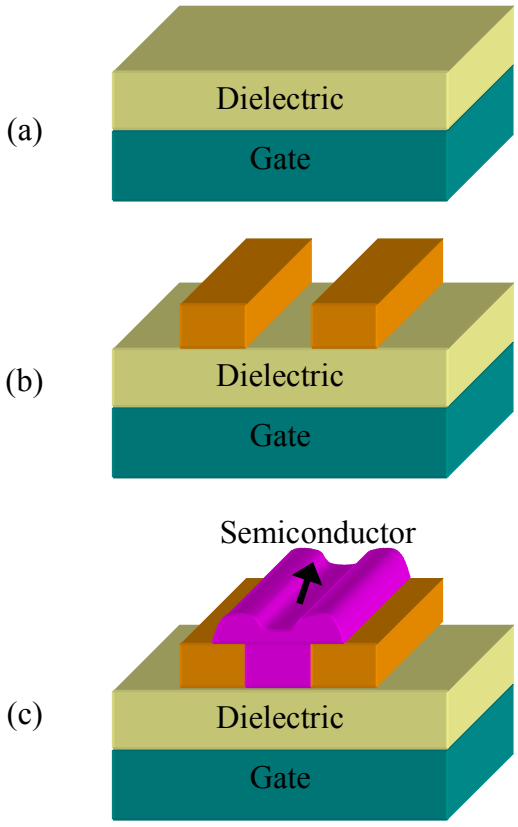


Fig. 2.5 The fabrication process of bottom-contact transistors; (a) dielectric surface cleaning (b) metal electrodes deposition and surface treatment by self-assembled monolayer (c) semiconductor deposition

The substrate is a heavily doped p-type silicon substrate serving as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric layer (34.5 nF/cm^2). After the substrates were cleaned by acetone, methanol, and deionized water with ultra-sonication, they were treated with oxygen plasma (Fig. 2.5(a)). The e-beam evaporated electrodes comprised of a 2.5 nm Ti adhesion layer and a 35 nm Au layer. The electrodes were photolithographically patterned with channel widths (W) and lengths (L) of 200 and 4 μm, respectively. Prior to the PDI-$8CN_2$ deposition, three kinds of surface treatments were performed; HMDS only, ODT only, and HMDS followed by ODT (Fig. 2.5(b)). Surface treatment will be discussed in the next section. The final fabrication step was thermal deposition of a 45 nm PDI-$8CN_2$ film (Fig. 2.5(c)). The PDI-$8CN_2$ had previously been purified by separation on silica and multiple recrystallizations. During the deposition, the substrates were maintained at 100 °C with a base vacuum of 4.5×10^{-7} Torr to enhance the PDI-$8CN_2$ grain growth, and the deposition rate was 0.2-0.7 Å/s. The devices were characterized by the Agilent 4155C semiconductor parameter analyzer in a Desert Cryogenics vacuum probe station at a pressure of $\sim 1\times10^{-3}$ Torr and the sample was measured in darkness.

2.3.4 SURFACE MODIFICATION BY SELF-ASSEMBLED MONOLAYERS

In order to achieve the performance required for practical electronics, shorter channel lengths for transistors (< 10 μm) are required. The fabrication of such structures is best accomplished in the bottom-contact configuration, in which

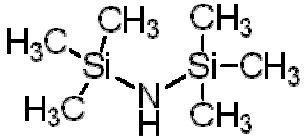
the source and drain electrodes are first defined and the semiconductor is deposited on top of the electrodes. However, most bottom-contact n-channel OFETs exhibit drastic erosion in electrical properties and reduced mobility versus the corresponding top-contact devices. This is as a result of the morphological changes in the semiconductor due to surface energy differences between the source and drain metal contacts and the dielectric. As a result, near the contact electrodes, organic molecules are not ordered well and this area degrades the device performance [42,43]. In addition, dipoles may be generated at the interface creating additional barriers to charge injection [30,86]. The influence of the contact becomes considerable as the channel length of an OTFT becomes smaller and it plays critical role in the performance of short channel length transistors. Most studies of bottom contact n-channel OFETs employ large channel length devices (≥ 50 μm) in which the contact injection requirements are reduced [36,37].

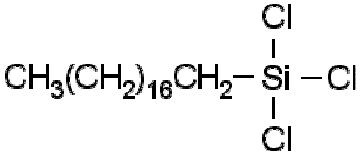
In order to minimize the interface problems, there are two approaches that can be employed. One is the use of a conducting polymer such as poly(3,4-ethylenedioxythiophene)/poly(styrene sulfonate) (PEDOT/PSS) and the other is utilization of suitable self-assembled monolayers (SAM). The use of a conducting polymer will be discussed in the next chapter. Self-assembled monolayers (SAMs) such as alkanethiols, aromatic thiols, silane-based materials have been extensively investigated because of their promising applications [80-85]. The use of SAMs can be classified into two ways for OFETs. One is the SAM treatment on the surface of gate dielectric, and the other is SAM treatment on the source/drain electrodes. Two commonly used agents for a self-assembled monolayer on top of SiO_2 are hexamethyldisilazane (HMDS) and

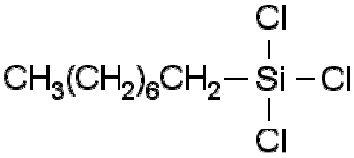
octadecyltrichlorosilane (OTS). These molecules are composed of two functional groups which are alkyl groups on one end and silane groups on the other end. When these molecules meet the surface of SiO_2, they react with the dangling hydroxyl group (-OH) at the surface and bind to SiO_2 through Si-O covalent bond contributed by their silane groups. Intermolecular interaction of Van der Waals forces enables the formation of well-ordered SAMs along the lateral direction. Therefore, all the alkyl groups align with each other in a head up fashion. The surface property of these alkyl head groups is hydrophobic, so that organic semiconducting layers can be ordered well. For example, a small amount of HMDS was poured in a bottle and the samples are placed below the lid of bottle. Nitrogen is filled in the bottle and stored in nitrogen. The samples were exposed to the HMDS vapor for 15 hours at room temperature in nitrogen. Treated samples were then cleaned with methanol and dried at 110 ºC for 1 min. Flash point of HMDS is 12 ºC, so that vapor pressure is enough to coat the SiO_2 surface with a trimethylsilyl monolayer which has lower surface energy at room temperature. In case of octyltrichlorosilane (OTS-8), the bottles were heated at 110 ºC for 15 min because vapor pressure is not enough to treat the samples at room temperature.

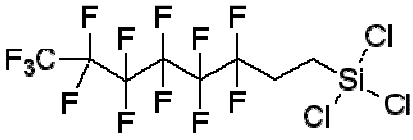
Thiol-based SAMs such as nitrobenzenethiol, octadecanethiol, and pentafluorobenzenethiol have also been employed for passivation of gold source and drain electrodes [39,41,42]. These molecules have thiol (-SH) groups on one end. When these molecules meet the surface of a metal such as gold and silver, thiol groups easily bind to the surface of the metal electrodes, so that these SAM agents modify the surface energy to facilitate charge carrier injection. As an example of the surface treatment of metal electrodes, octadecanethiol (ODT) or

hexadecanethiol (HDT) were dissolved in ethanol with a concentration of 5-10 mM. The samples were soaked for 1 hour in this solution. The wafers were then rinsed by additional ethanol twice and dried at 110 ºC for 1 min. For a special purpose, samples were treated with HMDS vapor to functionalize the oxide-based substrate/dielectric, followed by ODT solution-casting to functionalize the gold electrodes. The self-assembled monolayers can be fabricated with three methods; vapor evaporation, solution-casting, and spin-coating. Vapor evaporation is the best in terms of the quality of the SAM. Solution casting is the most common method used due to the ease in implementation and acceptable quality of SAM. Spin-coating is the fastest but not optimal for the formation of a SAM because of the short time duration of designated molecules remaining on the wafer surface as well as the lack of uniformity. Thus, the use of self-assembled monolayers (SAM) at the interface between the metal/insulator and the metal/semiconductor results in improved properties by lowering surface energy differences [38-40]. The examples of commonly used SAM agents are illustrated in Fig. 2.6.

(a) 

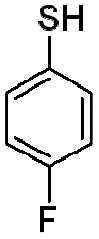
(b) 

(c) 

(d) 

(e) $CH_3-(CH_2)_{14}CH_2-SH$

(f) $CH_3-(CH_2)_{16}CH_2-SH$

(g) 

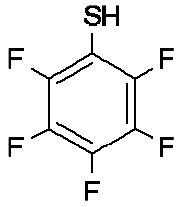
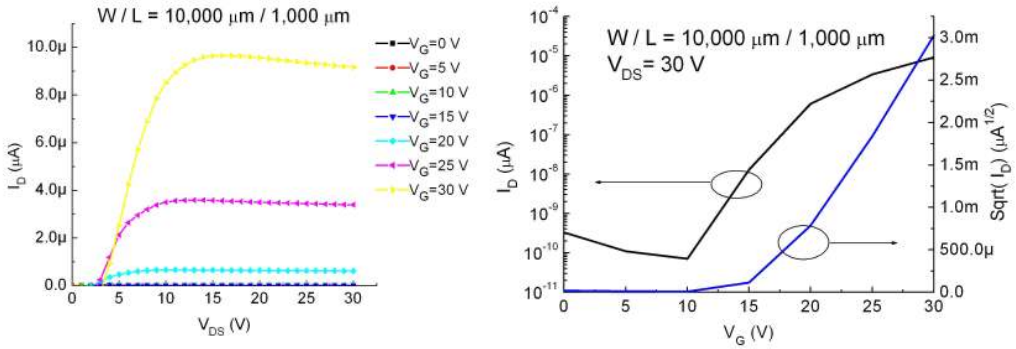
(h) 

Fig. 2.6 The common agents for the formation of a self-assembled monolayer on the dielectric surface and the metal electrode surface; (a) hexamethyldisilazane (b) octadecyltrichlorosilane (c) octyltrichlorosilane (d) perfluorooctyltrichlorosilane (e) hexadecanethiol (f) octadecanethiol (g) fluorothiophenol (h) pentafluorobenzenethiol

2.4 Results and discussion

2.4.1 DFHCO-4T TRANSISTORS

The output and transfer characteristics of DFHCO-4T transistors treated with HMDS are shown in Fig. 2.7. The device dimensions are 1000 μm for channel length and 10000 μm for channel width and the devices were measured in vacuum. The estimated saturation mobility, the threshold voltage, subthreshold swing, and I_{on}/I_{off} ratio (V_{DS} = 30 V) were 0.33 cm^2/Vs, 16.6 V, 2.5 V/decade and ~ 1 X 10^5, respectively. Some DFHCO-4T devices exhibit saturation mobility as high as ~ 0.65 cm^2 /Vs. Mobility summary of other DFHCO-4T transistors with different channel lengths are depicted in Table 2.2.



(a) (b)

Fig. 2.7 (a) Output and (b) transfer characteristics of 1 mm channel length (W / L = 10) top contact DFHCO-4T FETs with HMDS treatment in vacuum

Surface treatement	HMDS treatment				
Channel length (μm)	80	100	500	1090	1140
Channel width (μm)	800	1000	5000	10000	10000
Saturation regime mobility (cm^2/Vs) (V_{DS} = 60 V)	0.39	0.46	0.47	0.65	0.46

Table 2.2 Mobility summary of top-contact DFHCO-4T transistors with different channel lengths

A new approach to decouple the contact and channel resistance is described for the bottom-contact configuration in ref [79]. A similar approach for the top-contact configuration was first performed with DFHCO-4T devices. Fig. 2.8 shows the examples of a device with floating electrodes for measurement of contact resistance. The lengths of floating electrodes are 50 μm and the effective channel length, L_{eff}, is kept constant at 840 μm. The floating electrodes were evenly distributed along the channel. For example, total channel lengths of devices with one and two floating electrodes are 890 μm and 940 μm, respectively. The comparison of output characteristics with different number of floating electrodes at V_G = 35 V and the magnification of the output characteristics at the linear regime are shown in Fig. 2.9. The drain current is inversely proportional to the channel length in the linear and saturation regime. If the floating electrodes did not affect the channel conduction, the drain current

should proportionally decrease as the number of floating gates increase. This is due to the fact that other factors did not change and only the total channel length was increased.

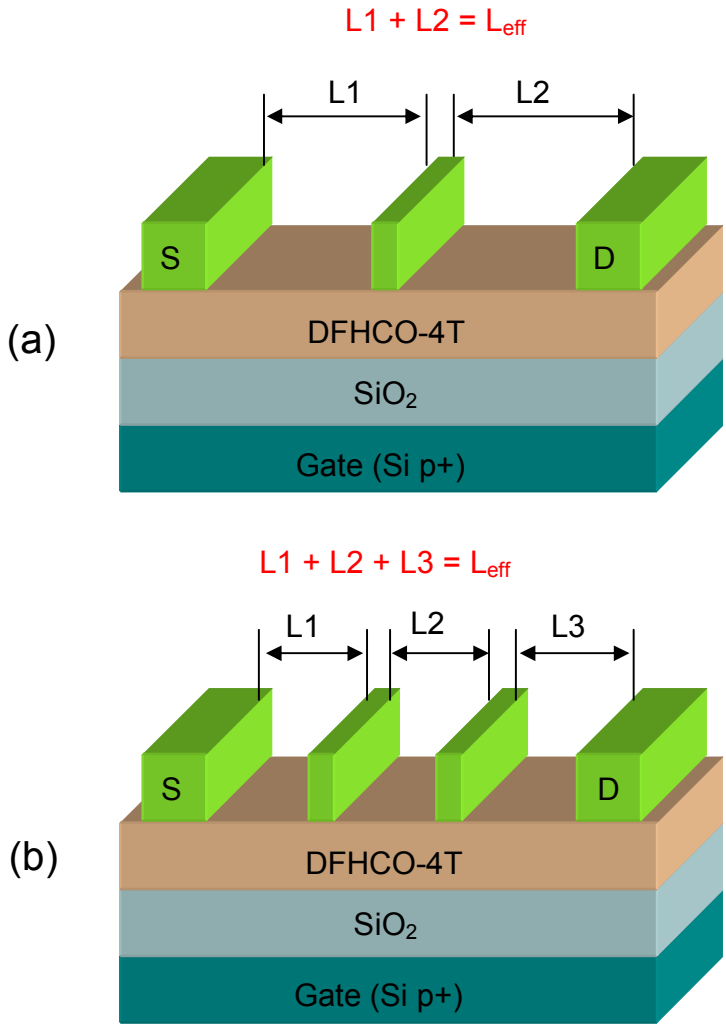


Fig. 2.8 Schematics of device geometry with (a) one and (b) two floating electrodes in the top-contact transistors. The effective channel length, Leff, was kept constant at 840 μm for all devices.

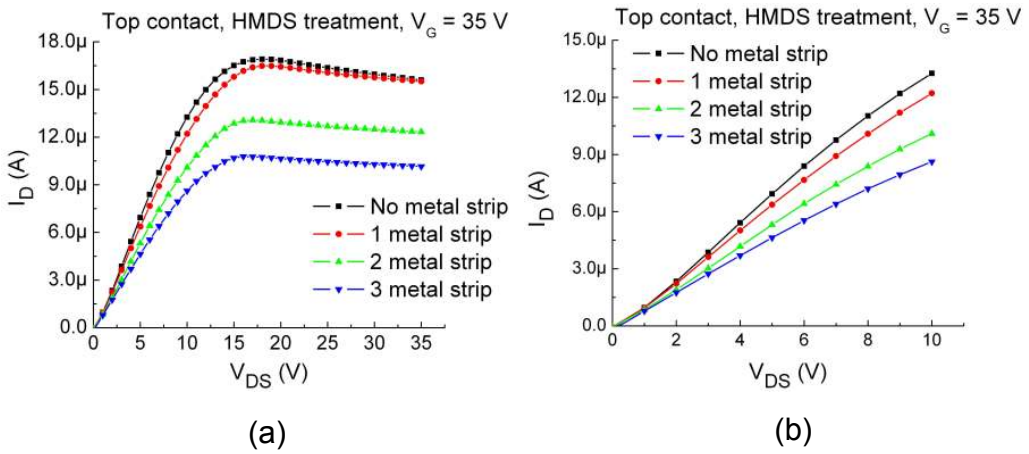


Fig. 2.9 (a) the comparison of output characteristics with devices having different numbers of floating electrodes at V_G = 35 V (b) the comparison of output characteristics in the linear regime with devices having different number of floating electrodes at V_G = 35 V

Fig 2.10 shows the fraction of the decrease in drain current (I_D) with respect to the number of floating electrodes between calculated I_D versus measured I_D at V_G = 35 V. I_D ratio can be defined as;

$$\mathbf{I_D\ ratio} = \frac{\mathbf{I_D\ (floating\ electrodes)}}{\mathbf{I_D\ (no\ floating\ electrodes)}}$$

As an example, devices having two floating electrodes, the calculated I_D ratio is 0.89 (840μm / 940μm ≈ 0.89) and the measured I_D ratio is 0.77 (3.02 μA (drain current of device with two floating electrodes) / 3.86 μA (drain current of device with no floating electrodes) ≈ 0.77). If the floating electrodes do not affect to the charge flow of the calculated I_D ratio and the measured I_D ratio should be the same because the drain current is only a function of channel length in this model. However, I_D ratio from calculation is higher than that from measurement as shown in Fig 2.10.

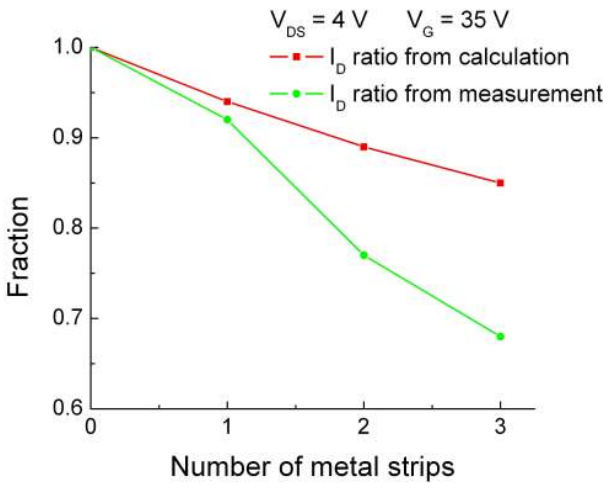


Fig. 2.10 The fraction of the decrease in drain current with respect to the number of floating electrodes between calculated I_D versus measured I_D for a linear regime (V_{DS} = 4 V) at V_G = 35 V. I_D ratio = I_D (floating electrodes) / I_D (no floating electrodes)

There have been reports that the fabrication of metal-on-organic semiconductor interfaces can lead to the penetration of metal into the semiconductor during deposition [87-89]. We assume that the charge density is uniform on the semiconductor layer and floating electrodes penetrate into the semiconductor layer. Accordingly, additional voltage drop at the penetrated metal/semiconductor interfaces results in the additional decrease of current. The number of floating electrodes was varied from 0 to 3 so that the number of contact interfaces was 2 to 8, increasing by 2 for each floating electrode. Since the conductivity of the metal electrode is many orders of magnitude higher than that of the semiconductor, all the carriers flowing through a channel will flow through an electrode.

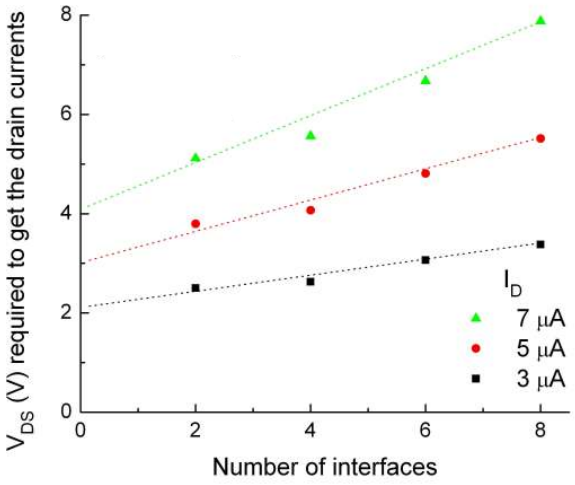


Fig. 2.11 Required V_{DS} for the given drain current versus the number of metal/semiconductor interfaces.

For the sake of correlation between the voltage drop and the number of interfaces, the drain voltages (V_{DS}) to get the same drain current with respect to the devices which have different numbers of floating electrodes were extrapolated in the linear regime. V_{DS} increases as the number of interfaces of the devices increase due to the potential drop at the interface as shown in Fig. 2.11. The y intercept of the extrapolated line is the drain voltage (V_{DS0}) of the intrinsic device which has no contact effect in order to get the same drain current with other devices. In the linear regime, the channel resistance can be calculated by simple ohm's law ($R = V_{DS0} / I$). The contact resistance can be extracted by comparison between the total resistance and channel resistance. When V_{DS} = 5 V, the approximated channel resistance and contact resistance are 560 kΩ and 160 kΩ, respectively. The fraction of the channel resistance ($R_{Fraction} = R_{Channel} / R_{Channel+contact}$) is about 80%. Therefore, the contact resistance is not a major

concern for top contact devices. To confirm the value of contact resistance by this method, the devices with same channel widths and different channel lengths were fabricated [77,78]. The contact resistance was calculated at the same condition (V_{DS} = 5 V) as shown Fig. 2.12 and the approximated contact resistance is 154 kΩ which is within 4% of error in comparison with the value obtained from the floating electrode method. Fig. 2.13 shows the gate voltage dependence with respect to the channel and contact resistance. The contact resistance is decreased with increasing gate voltage due to the increased gate bias which can reduce the barrier at the metal / semiconductor interface [11]. The channel resistance is also decreased because the increased field-induced charges are filled up traps [12]. The fraction of the channel resistance is maintained as a flat line throughout the gate change in gate voltage. This shows that contact resistance can be reduced by the increase of induced carrier densities in the channel.

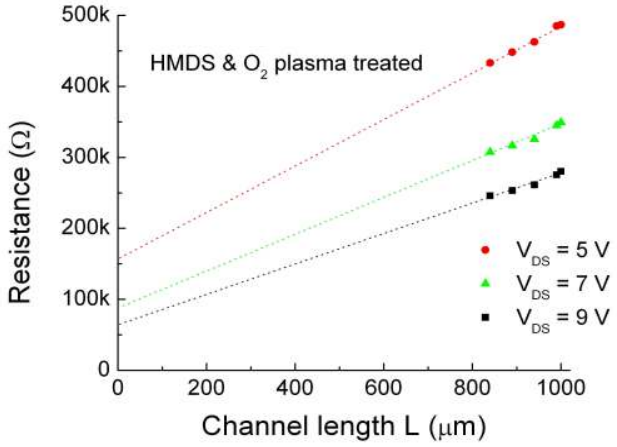


Fig. 2.12 The calculation of contact resistance by the correlation of the total resistance with respect to different channel length devices. The approximated contact resistance is 154 kΩ at V_{DS} = 5 V

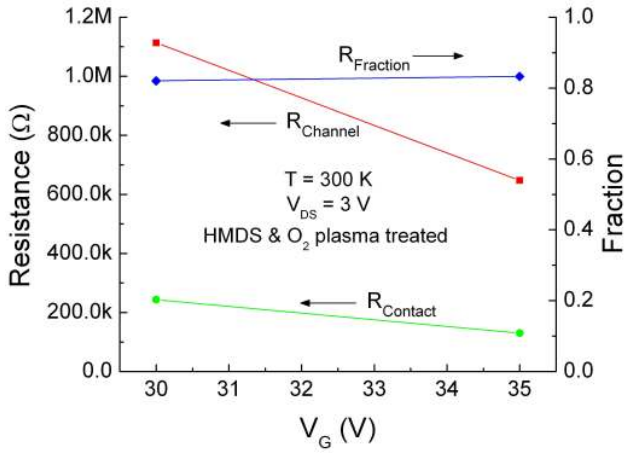


Fig. 2.13 Gate voltage dependence with respect to the channel and contact resistance at V_{DS} = 3 V. $R_{Fraction} = R_{Channel} / R_{Channel+contact}$

2.4.2 PDI-8CN_2 TRANSISTORS

In bottom contact devices, there is a disordered region at the interface between the metal and gate insulator interface that affects mobility. The use of self-assembled monolayers (SAM) at the interface between the metal/insulator and the semiconductor results in improved properties by lowering surface energy differences. Therefore, three kinds of surface treatments were performed; HMDS only, ODT only, and HMDS followed by ODT prior to the deposition of PDI-8CN_2. The transfer and output characteristics of representative PDI-8CN_2 transistors treated with both HMDS and ODT are shown in Fig. 2.14(a) and Fig. 2.14(b), respectively.

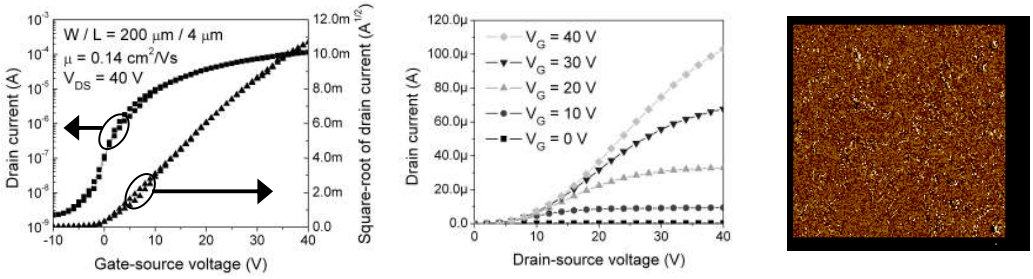


Fig. 2.14 (a) Transfer characteristics of 4 μm channel length (W / L = 50) OFETs with HMDS+ODT SiO_2 treatment at V_D = 40 V, measured in a vacuum of ~2 X 10^{-3} Torr, calculated mobility = 0.14 cm^2/Vs, V_{TH} = 1.64 V, I_{on}/I_{off} (V_{DS} = 40 V, V_G = 0 ~ 40 V) = 1.2 X 10^3. The gate bias was swept from negative to positive voltage. (b) Output characteristics of 4 μm channel length (W / L = 50) OFETs with HMDS+ODT SiO_2 treatment measured in a ~2x10^{-3} vacuum atmosphere (c) atomic force microscopic (AFM) image of a sublimed PDI-8CN_2 film of the dimension of 5 μm X 5 μm with 512 points per line. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 88, 082104 (2006). Copyright 2006, American Institute of Physics.

Noticeable hysteresis was not found in the transfer characteristics; however, the current was still injection limited in the low drain voltage region despite the ODT treatment. The saturation mobility, the threshold voltage, and subthreshold swing are 0.14 cm2/Vs, 1.6 V, and 2.0 V/decade, respectively. I_{on}/I_{off} ratio (V_{DS} = 40 V, V_G = 0 / 40 V) is 1.2x10^3 and I_{on}/I_{off} ratio (V_{DS} = 40 V, V_G = -10 / 40 V) is 5.7x10^4. Such I_{on}/I_{off} ratios are typical of cyanated PDI semiconductors. The surface morphology of the PDI-8CN_2 film was observed by an atomic force microscopic (AFM) image (Fig. 2.14(c)). The scale of the AFM image was 5 μm X 5 μm with 512 points per line and the molecule of PDI-8CN_2 is a rod-like structure. The mean length and width were approximately 750 nm and 230 nm, respectively.

Condition	Mobility (cm^2/Vs)	V_{TH} (V)	I_{on} / I_{off} ratio (V_{DS} = 40 V) (V_g = 0~40 V)
As-prepared	3.9×10^{-2}	-1.9	1.1×10^{2}
HMDS treatment	4.4×10^{-2}	2.0	2.8×10^{3}
Octadecanethiol treatment	7.5×10^{-2}	-6.4	3.7×10^{1}
HMDS + Octadecanethiol	0.14	1.6	1.2×10^{3}

Table 2.3 Comparison of mobility, threshold voltage, and on/off current ratio for OFETs with various surface treatments. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 88, 082104 (2006). Copyright 2006, American Institute of Physics.

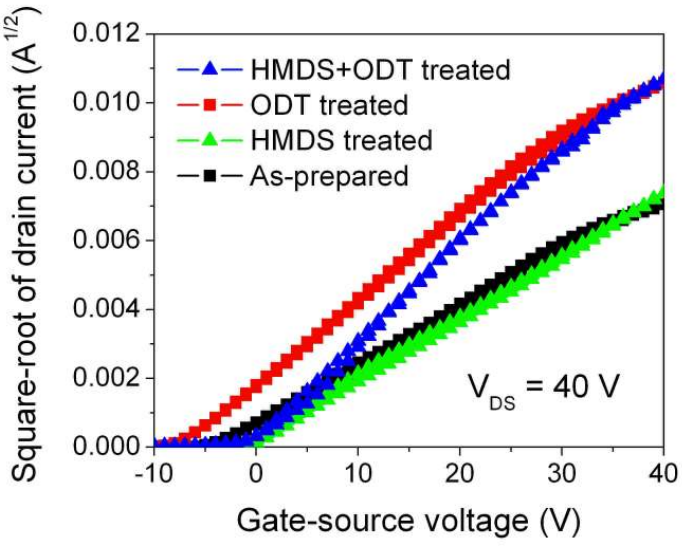


Fig. 2.15 Square-root of drain current versus gate voltage characteristics at a source/drain voltage equal to 40V for as-prepared (black square), HMDS-treated (green triangle), ODT-treated (red square), and HMDS + ODT treated (blue triangle) FETs with channel length L = 4 μm and width W = 200 μm. The gate bias was swept from negative to positive voltage. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 88, 082104 (2006). Copyright 2006, American Institute of Physics.

Fig. 2.15 shows $\sqrt{I_D}$ versus V_G plots at a source-drain voltage of 40 V for devices fabricated with four different surface treatments. No noticeable improvement of mobility is observed on HMDS treated SiO_2 surface functionalized samples. However mobility is enhanced by about one order of magnitude for ODT-treated (Au surface functionalized) samples. The off-current of the ODT-treated samples is greater than that of the HMDS-treated samples by approximately two orders of magnitude, which results in a low Ion/Ioff ratio for the ODT-treated samples. The mobility, threshold voltage, and current on/off ratio for OFETs fabricated with various surface treatments are summarized in Table 2.3. The threshold voltage is slightly positive for HMDS-treated and HMDS + ODT treated devices. If additional charge is created on the SiO_2 surface by surface treatment, the charge carrier concentration can be influenced, thus affecting the threshold voltage [40].

The work function levels of general contact metals such as Au (~ 5.1 eV), or Ag (~ 4.7 eV) are more favorable for hole injection than electron injection in typical organic semiconductors. The trials with low work function metals such as Ca (~ 2.9 eV), or Mg (~ 3.6 eV) had been unsuccessful for the applications in ambient because of their susceptibility to oxidation and formation of complexes. Nevertheless, the use of low work function metals is still favorable for n-channel OFETs to make ohmic contacts between the n-channel organic semiconductor and the electrodes. Accordingly, two kinds of general contact metals (Au and Ag) are compared in the PDI-$8CN_2$ OFETs. The substrate was a heavily doped p-type silicon substrate serving as the gate electrode. The gate dielectric was composed of double layers, with the confidential polymer dielectric solutions

called as P121 or P139 (supported by OrganicID) being directly spun cast on thermally grown SiO_2.

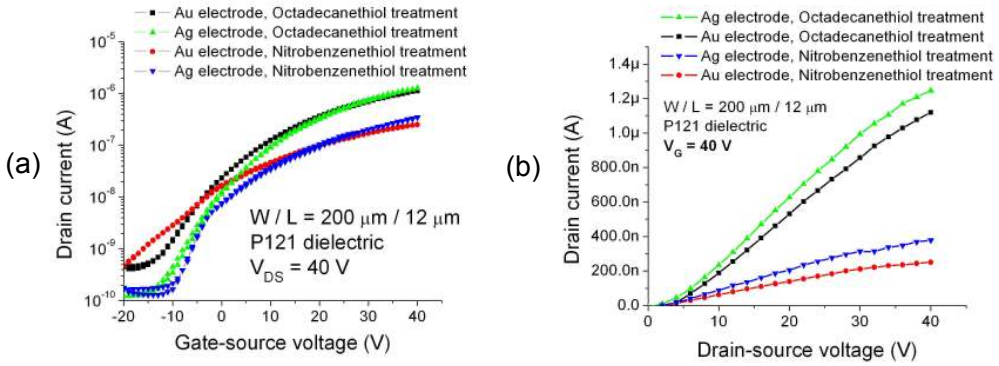


Fig. 2.16 The comparison of characteristics of 12 μm channel length (W / L = 16.7) OFETs with different metal electrodes and surface treatments. Sublimed semiconductor was PDI-$8CN_2$ and the gate dielectric is composed of double layers which are SiO_2 and a confidential polymer dielectric called as P121. (a) Transfer characteristics of OFETs at V_{DS} = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), Au electrodes with NBT treatment (red circle), and Ag electrodes with NBT treatment (blue inverted triangle). (b) output characteristics of OFETs at V_G = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), Au electrodes with NBT treatment (red circle), and Ag electrodes with NBT treatment (blue inverted triangle)

Fig. 2.16 and Fig. 2.17 show the comparison of characteristics of 12 μm channel length (W / L = 16.7) OFETs with different metal electrodes and the electrode surface treatments. The work function of Au was approximately 0.4-0.6 eV higher than that of silver (Ag) and the HOMO and LUMO level of PDI-$8CN_2$ are 7.1 eV and 4.3 eV, respectively. As a result, the height of the electron injection barrier between PDI-$8CN_2$ and Au is higher than that between PDI-$8CN_2$ and Ag. Therefore, facilitating the electron injection is achieved through

the use of Ag electrodes, so that the mobility of devices with Ag electrodes is higher. Mobility summary of other PDI-8CN$_2$ OFETs with different metals and surface treatments is depicted in Table 2.4.

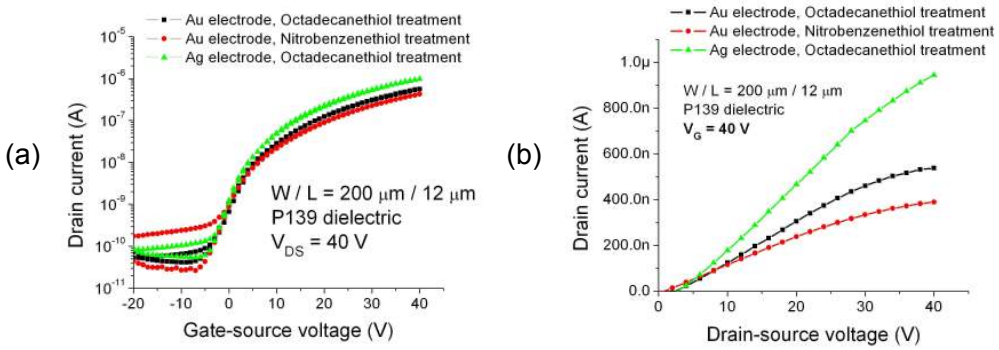


Fig. 2.17 The comparison of characteristics of 12 μm channel length (W / L = 16.7) OFETs with different metal electrodes and surface treatments. Sublimed semiconductor was PDI-8CN$_2$ and the gate dielectric was composed of double layers which were SiO$_2$ and confidential polymer dielectric called as P139. (a) Transfer characteristics of OFETs at V_{DS} = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), and Au electrodes with NBT treatment (red circle). (b) output characteristics of OFETs at V_G = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), and Au electrodes with NBT treatment (red circle)

Moreover, it is observed that ODT treatment is more effective than nitrobenzenethiol (NBT) treatment in terms of good charge carrier injection for the PDI-8CN$_2$ OFETs. Alkanethiols are known to decrease the work functions of metals due to the shift of vacuum energy levels [90-92], so that it is ideal for use in n-channel OFETs in order to make an ohmic contact. In addition, the dipole moment between Ag and sulfur (S) in thiol is larger than that between Au and S [90]. It may also help to decrease the work function of the metal further

and facilitate charge injection into the PDI-8CN_2 layer. Same effect was observed with shorter channel length devices (L= 4 μm) as shown Fig. 2.18.

W / L (μm)	200 / 12			
$C_{Dielectric}$ (F/cm^2) (SiO_2 + polymer)	7.9×10^{-9}			
Electrode material	Au		Ag	
Electrode treatment	ODT	NBT	ODT	NBT
Mobility (cm^2/Vs)	9.6×10^{-3}	1.5×10^{-3}	1.2×10^{-2}	2.5×10^{-3}

Table 2.4 Comparison of mobilities for OTFTs having different metal electrodes and electrode surface treatments

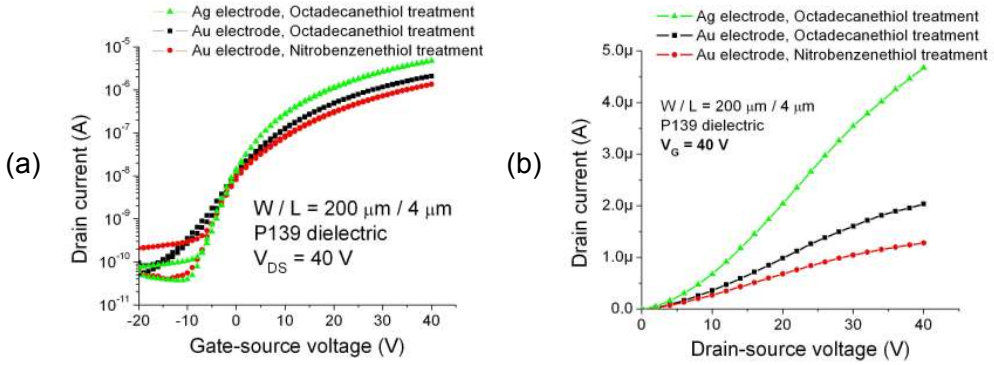


Fig. 2.18 The comparison of characteristics of 4 μm channel length (W / L = 50) OFETs with different metal electrodes and surface treatments. Sublimed semiconductor was PDI-8CN_2 and the gate dielectric was composed of double layers which were SiO_2 and a confidential polymer dielectric called as P139. (a) Transfer characteristics of OFETs at V_{DS} = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), and Au electrodes with NBT treatment (red circle). (b) output characteristics of OFETs at V_G = 40 V for Au electrodes with ODT treatment (black square), Ag electrodes with ODT treatment (green triangle), and Au electrodes with NBT treatment (red circle)

2.5 Conclusion

Top-contact DFHCO-4T thin film transistors and bottom-contact PDI-$8CN_2$ transistors were demonstrated. For the top-contact DFHCO-4T OFETs, the estimated saturation mobility, the threshold voltage, subthreshold swing, and I_{on}/I_{off} ratio (V_{DS} = 30 V) were 0.33 cm^2/Vs, 16.6 V, 2.5 V/decade and ~ 1 X 10^5, respectively. The floating electrode method was applied to determine the contact resistance in top-contact DFHCO-4T OFETs. It is shown that the contact resistance is not a major problem for large size devices in the top-contact configuration. We have described the electrical characteristics of bottom-contact organic field-effect transistors fabricated with another promising n-type semiconductor, PDI-$8CN_2$. The effect of electrode/dielectric surface treatment on the response of these devices was also examined, with a combination of ODT (Au electrode functionalization) and HMDS (SiO_2 dielectric functionalization) yielding maximum mobility in the PDI-$8CN_2$ devices. Noticeable hysteresis was not observed. The saturation mobility, threshold voltage, sub-threshold swing, and Ion/Ioff ratio (V_{DS} = 40V, V_G = 0 ~ 40 V) are 0.14 cm^2/Vs, 1.6 V, 2.0 V/decade, and 1.2 X 10^3, respectively. Ion/Ioff ratio (V_{DS} = 40 V, V_G = -10 ~ 40 V) is $5.7x10^4$. Different metal electrodes and electrode surface treatments were compared in the PDI-$8CN_2$ OFETs and the use of lower work function metal (Ag) and alkanethiol surface treatment helped in improving the performance of n-channel OFETs.

CHAPTER 3 CONDUCTING POLYMER CONTACTS AND POLYMER GATE DIELECTRICS

3.1 Introduction

Polymer electronics have been considered a promising technology requiring low cost mass production and solution processible properties for applications such as printed circuits on flexible substrates [93]. All organic electronic devices with high performance being the goal, there are three aspects of organic transistors; semiconductors, electrodes, and gate dielectric which are equally important for the realization of this goal.

The field of conducting polymers has been widely researched. Among the many conducting polymers such as derivatives of polythiophenes, polyanilines, polypyrroles, and polyphenylenes, poly(3,4-ethylenedioxythiophene)/poly(styrene sulfonate) (PEDOT/PSS) is one of the most successful conducting polymers. It is developed by Bayer AG research laboratories in Germany and the commercial trade name is Baytron®. The chemical structure of PEDOT/PSS is shown in Fig. 3.1 and it is a water-soluble polymer with a low oxidation potential, moderate bandgap (1.6 eV), good film formation properties, high visible light transmission, and high stability. Solution-based PEDOT/PSS can be deposited by spin-coating or by using printing techniques and it has been already exploited for applications such as organic LEDs, organic solar cells, and electrodes in OTFTs [94-98].

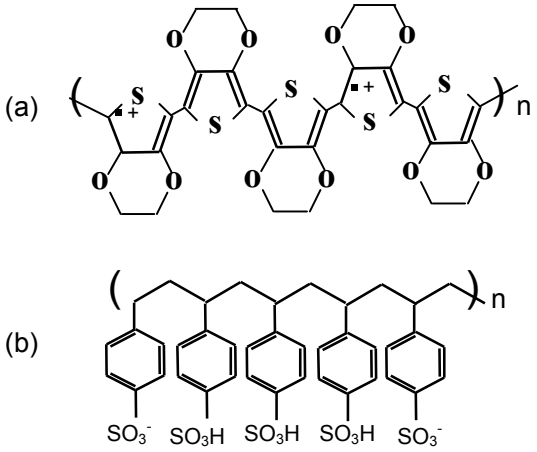


Fig. 3.1 The chemical structures of (a) PEDOT and (b) PSS

The major challenges of polymer electrodes are their low conductivities compared to inorganic compounds. The high resistance of the polymer electrodes lowers the performance of devices and Joule heating generated by the current flow through the polymer electrodes degrades the lifetime of these devices. One of the significant properties of conducting polymers is that the electrical conductivity can be tuned by chemical manipulation of the polymer backbone, by blending with other organic compounds [98-100]. Recent work by Ouyang *et al.*, demonstrated that conductivity enhancement of PEDOT/PSS can be achieved by adding a compound with two or more polar groups [100,101]. We exploited this effect in the fabrication of OFETs and the contact resistances were measured with respect to various conditions of the electrodes. These measurements can ensure that the use of a conducting polymer enables to reduce the contact problems in the bottom contact configuration.

Polymer dielectrics are another important issue in OFETs. Polymer dielectrics are significantly different from inorganic dielectrics. Thermally

grown SiO_2 is the widely used in organic dielectric and it is a chemically stable. However, polymer dielectrics give rise to a number of effects in OFETs due to the mismatch of surface energies and due to their reactivity with organic semiconductors. The dielectric can affect the morphology of the semiconducting layer and the molecular ordering. The polarity of the dielectric can also play a role, affecting the distribution of electronic states and local morphology on the semiconducting layer. The interface roughness of polymer dielectrics can potentially be influenced by heat treatment and from the use of solvents as compared to the inorganic dielectrics. Therefore, the influence of a polymer dielectric on the carrier transport and the performance of OFETs is much more significant. Nevertheless, polymer dielectrics have great potential for low cost fabrication on large area, flexible substrates [28,102-104]. Among the solution processible dielectric materials such as polypropylene, CYTOP™, polyvinylalcohol, polyvinylphenol, and polymethyl-methacrylate, poly(4-vinyl phenol) (PVP) is one of the most common and successful polymer dielectric. Accordingly, the PDI-$8CN_2$ transistors with PVP as the gate dielectric were fabricated and the electrical characteristics of OFETs were investigated. PDI-$8CN_2$ transistors with different surface treatments on the gate dielectric were compared. The fabrication of a simple organic complementary circuit on PVP dielectric will be also discussed in the chapter 4. The device characterization was done on the Agilent 4155C semiconductor parameter analyzer in a Desert Cryogenics vacuum probe station at a pressure of $\sim 1\times10^{-3}$ Torr and the sample was held in darkness during the measurement. To measure the capacitance of the PVP dielectric layer, a HP 4284A precision LCR meter was used.

3.2 Poly(3,4-ethylenedioxythiophene) : poly(styrene sulfonate) as the conducting polymer

3.2.1 PDI-8CN_2 TRANSISTORS WITH PEDOT/PSS ELECTRODES

There are typically two solutions to minimize the interface problems in bottom contact devices. One is the utilization of suitable SAM treatment and the other is the use of a conducting polymer. The work function of a conducting polymer does not have a large surface electronic component which causes the vacuum level shift in comparison with that of inorganic metals such as Au [105]. Firstly, the mobility and the contact resistance are compared to show the advantage of using a conducting polymer. PDI-8CN_2 OFETs with Au electrodes are fabricated for comparison and those with PEDOT/PSS electrodes are also fabricated. PDI-8CN_2 OFETs with Au electrodes have a typical bottom contact structure. A highly doped p-type Si substrate is used as a gate with 100nm of thermally grown SiO_2 as the gate dielectric. The electrodes are patterned using conventional photolithography. 2.5 nm of Ti as an adhesion layer and 35 nm of Au are deposited by e-beam evaporation. HMDS treatment is performed on the sample. Finally, PDI-8CN_2 OFETs is thermally evaporated. The substrates were maintained at 100 ºC to enhance the PDI-8CN_2 grain growth. Deposition rate was 0.1~0.6 Å/s. The channel width and length are 200 μm and 4 μm, respectively.

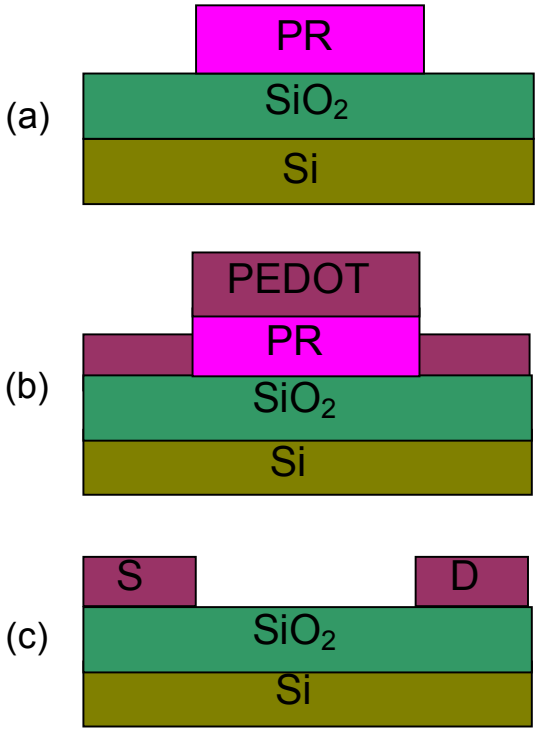


Fig. 3.2 The fabrication process of bottom contact transistors with PEDOT/PSS electrodes. (a) the electrodes are photolithographically patterned (b) After O_2 plasma, making the dielectric surface hydrophilic, PEDOT/PSS solution was spin-coated, so that hydrophilic PEDOT/PSS solution attached to the dielectric surface (c) the photoresist was removed by lift-off

The fabrication process of bottom contact OFET with PEDOT/PSS electrodes is illustrated in Fig. 3.2. The gate and gate dielectric are same as these used for devices with Au electrodes. The electrodes are photolithographically patterned. O_2 plasma was performed to make the dielectric surface hydrophilic. The power and time of O_2 plasma were 80 W and 11 sec, respectively. PEDOT/PSS solution was then spin-coated on the sample. The spin speed and time were 2500 rpm and 40 sec, respectively. Accordingly,

hydrophilic PEDOT/PSS solution attached to the dielectric surface. After the samples were annealed at 85 ºC for 15 min, the photoresist was removed using lift-off followed by HMDS treatment. The final step was thermal deposition of PDI-8CN$_2$ at a rate of 0.1~0.6 Å/s and substrate temperature of 100 ºC.

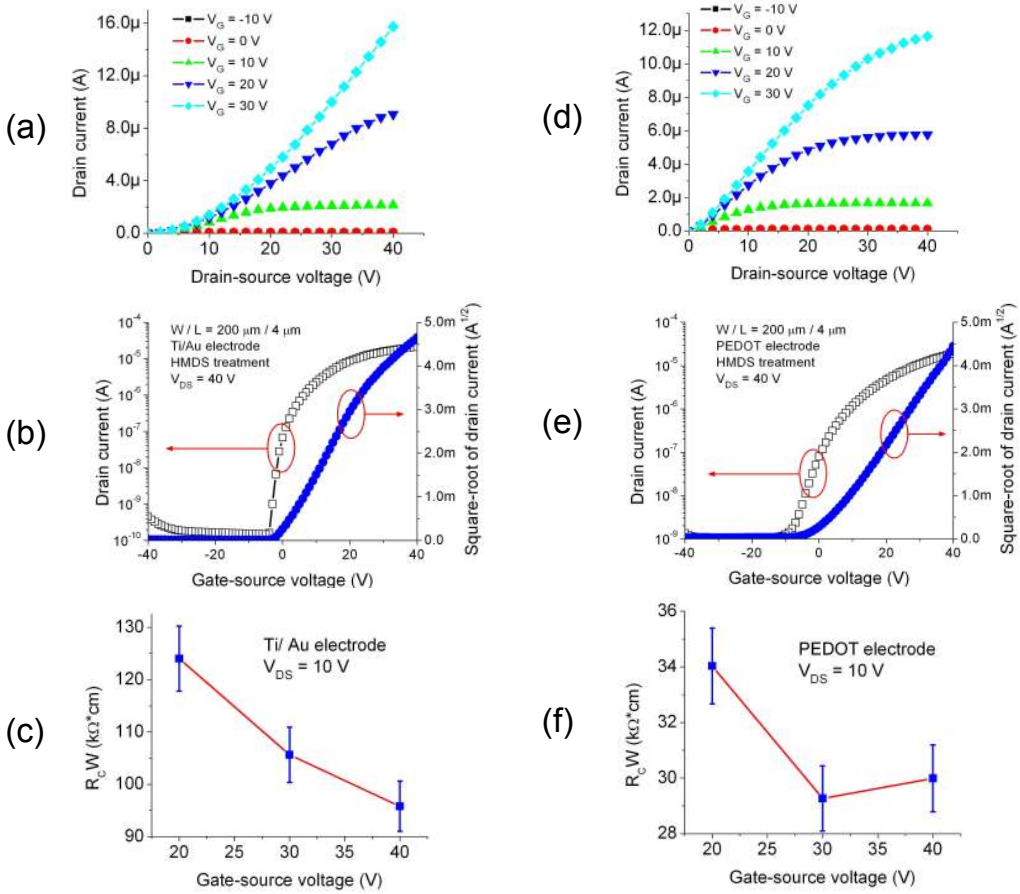


Fig. 3.3 Characteristics of PDI-8CN$_2$ OFETs with Au electrodes; (a) output characteristics (b) transfer characteristics of (c) contact resistance versus gate voltage at V_{DS} = 10 V. Characteristics of PDI-8CN$_2$ OFETs with PEDOT/PSS electrodes; (d) output characteristics (e) transfer characteristics of (f) contact resistance versus gate voltage at V_{DS} = 10 V

The comparison of PDI-8CN_2 OFETs characteristics between Au electrodes and PEDOT/PSS electrodes are shown in Fig. 3.3. The output characteristics of devices with Au electrodes indicate superlinear behavior of the drain current in the linear regime due to the contact effect as shown in Fig. 3.4. Several studies have shown that injection barriers are reduced when PEDOT/PSS electrodes are used instead of Au electrodes [105]. Therefore, the utilization of PEDOT/PSS electrodes may help to inject the charge carrier, so that the magnitude of drain current is larger in PDI-8CN_2 OFETs with PEDOT/PSS electrodes (Fig. 3.4). While the contact resistance is independent of channel length, the channel resistance is proportional to the channel length. Consequently, the relative influence of the contact resistance increases as the channel length is reduced. Since the channel length is only 4 μm, the influence of contact resistance should be large with respect to the devices having long channel lengths. Fig. 3.3(c) and (f) show the contact resistance with respect to different gate voltages for both types of devices. In order to measure the contact resistance, we measured the total resistance with different channel length devices and then performed an extrapolation. It is shown that the devices with Au electrodes have higher contact resistance than that with PEDOT electrodes. Contact resistance also decreases with increasing gate voltage due to the increase in carrier density in the channel and near the contacts. However, the electrical conductivity of PEDOT/PSS is several orders of magnitude lower than that of Au and it degrades the performance of the OTFT. The mobility, Ion/off ratio, and the contact resistance for each of the devices are summarized in Table 3.1.

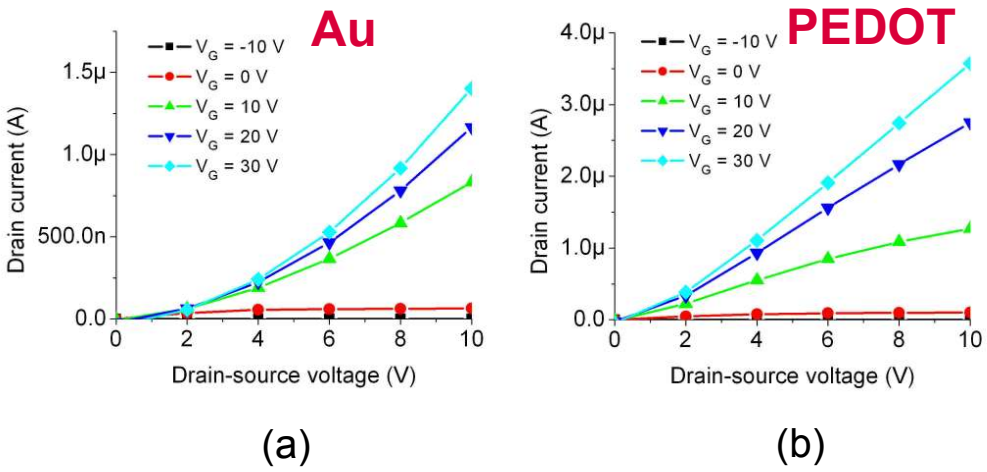


Fig. 3.4 Output characteristics of PDI-8CN_2 OFETs with (a) Au electrodes and (b) PEDOT/PSS electrodes at the linear regime

Electrodes		Au	PEDOT
Saturation regime μ (cm^2/Vs)		2.4×10^{-2}	1.9×10^{-2}
Linear regime μ (cm^2/Vs)		3.6×10^{-3}	8.7×10^{-3}
Ion/off ratio		$> 10^5$	$> 10^4$
$R_C W$ (KΩ·cm)	V_G = 20 V	124.0	34.0
	V_G = 30 V	105.6	29.2
	V_G = 40 V	95.8	29.8

Table 3.1 Summary comparing the mobility, current on/off ratio, and contact resistances between PDI-8CN_2 OFETs with Au electrodes and PDI-8CN_2 OFETs with PEDOT/PSS electrodes

3.2.2 PDI-8CN_2 TRANSISTORS WITH PEDOT/PSS COATED GOLD ELECTRODES

It is well known that the conductivity of metal electrodes is much higher than that of conducting polymers. Keeping in mind the concerns of the injection barrier and morphological aspects as well, the use of a conducting polymer is better. Therefore, we coated PEDOT/PSS on Au electrodes. First, Au electrodes are prepared on the Si/SiO_2 substrate. O_2 plasma treatment is performed to make the surface hydrophilic. HMDS treatment is then performed to change the nature of the surface of the gate dielectric making it hydrophilic. After that, the PEDOT/PSS solution is spin-coated, so that the PEDOT/PSS only attaches to the surface of Au electrodes because the surface of gate dielectric is hydrophobic. Finally, PDI-8CN_2 was thermally deposited at a rate of 0.1~0.6 Å/s with the substrate temperature maintained at 100 ºC. The device dimensions are the same.

Fig 3.5 shows the output and contact resistance characteristics of PDI-8CN_2 OFETs using PEDOT/PSS coated Au electrodes. It shows that contact resistance decreases with increasing gate voltage. The thickness of the coated PEDOT/PSS layer on the Au electrodes was approximately 500 Å. Saturation and linear regime mobility of these devices were further increased to $4.3x10^{-2}$ cm^2/Vs and $1.2x10^{-2}$ cm^2/Vs, respectively. This is one order of magnitude higher linear mobility with respect to the value obtained Au electrodes only. Ion/off ratio was more than 10^5. In comparison with devices using only Au electrodes, the contact resistance at 30 V, gate voltage was also greatly decreased

from 105 KΩ·cm to 19 KΩ·cm. This technique is a simple and effective way to reduce the contact resistance in bottom contact devices.

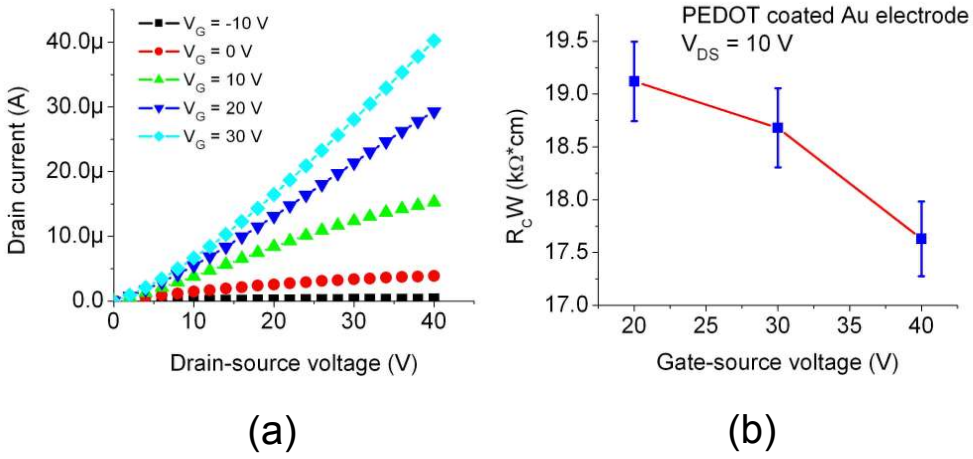


Fig. 3.5 (a) output characteristics of PDI-8CN$_2$ OFETs with PEDOT/PSS coated Au electrodes (b) contact resistance versus gate voltage at V_{DS} = 10 V

3.2.3 PDI-8CN$_2$ TRANSISTORS WITH ETHYLENE GLYCOL TREATED PEDOT/PSS ELECTRODES

To realize low cost fabrication on flexible substrates, the conducting polymer should be solely applied to the electrodes without any need to set additional deposition equipment. Therefore, the modifications to conducting polymers have been investigated for enhancing their conductivity by adding organic compounds such as methyl sulfoxide, N,N-dimethylformamide, glycerol, and ethylene glycol [98-100,106]. Among the many reports of various such compounds, ethylene glycol was chosen as an adding compound due to the ease

of application to the OFETs. When ethylene glycol (EG) was added to the PEDOT/PSS solution, the post annealing process did not play an important role in the enhancement of conductivity. Immersing the PEDOT/PSS film into the ethylene glycol also gives rise to conductivity enhancement [101]. Adding ethylene glycol in the PEDOT/PSS may transfer the resonant structure of the PEDOT chain from the benzoid structure to the quinoid structure. This conformational change results in stronger interchain interaction among the PEDOT chains, so that it facilitates the charge carrier flow. Both structures are shown in Fig. 3.6.

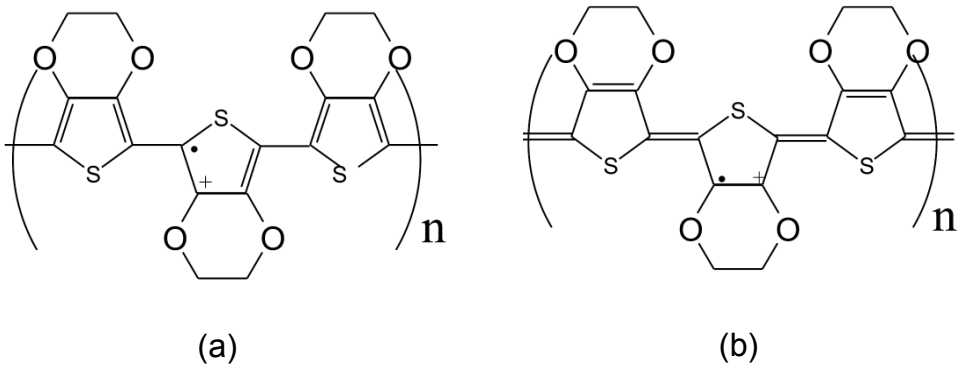


Fig. 3.6 (a) benzoid structure (b) quinoid structure. Unpaired electron and positive charge on the PEDOTchain are are represented as the dot and plus sign, respectively. Adapted from ref. [100]

To clearly confirm this improvement, the conductivity of the PEDOT/PSS electrodes was estimated. The conductivity σ was given by the following equation;

$$\sigma = \frac{1}{R} \times \frac{l}{A}$$

where A and *l* are the cross section of the electrode and the length, respectively. The resistance R was obtained from the inverse of the I-V slope as shown in Fig. 3.7. PEDOT/PSS electrodes are patterned by lift-off process on Si/SiO2 substrates as shown in the inset of Fig. 3.7. The results of these calculations indicated that the conductivity of ethylene glycol-treated PEDOT (EG-PEDOT) electrodes shows more than a 40 fold increase, from 0.15 to 6.5 S/cm. A numbers of studies have reported that conductivity enhancement of more than two orders of magnitude can be achieved on treatment with ethylene glycol [100,101].

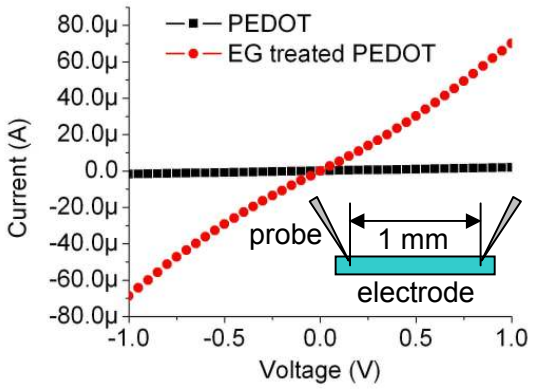


Fig. 3.7 Comparison of I-V characteristics between untreated PEDOT electrodes and ethylene glycol-treated PEDOT (EG-PEDOT) electrodes

Therefore, we effectively utilized this effect in the PDI-8CN_2 OFETs fabricated by the conventional lift-off process. A heavily doped p-type silicon substrate serves as the gate electrode and 100 nm of thermally grown SiO_2 was used as the dielectric layer. The photoresisit was patterned by photolithography. Oxygen plasma was performed to make the dielectric surface hydrophilic.

PEDOT/PSS solution was spun on patterned photoresist and cured at 85 °C for 15 min. The samples were then immersed in the ethylene glycol for 3 min and cleaned. Annealing of the sample was performed at 85 °C for 10 min. Photoresist was then removed by lift-off. The channel width and length are 200 μm and 4 μm, respectively.

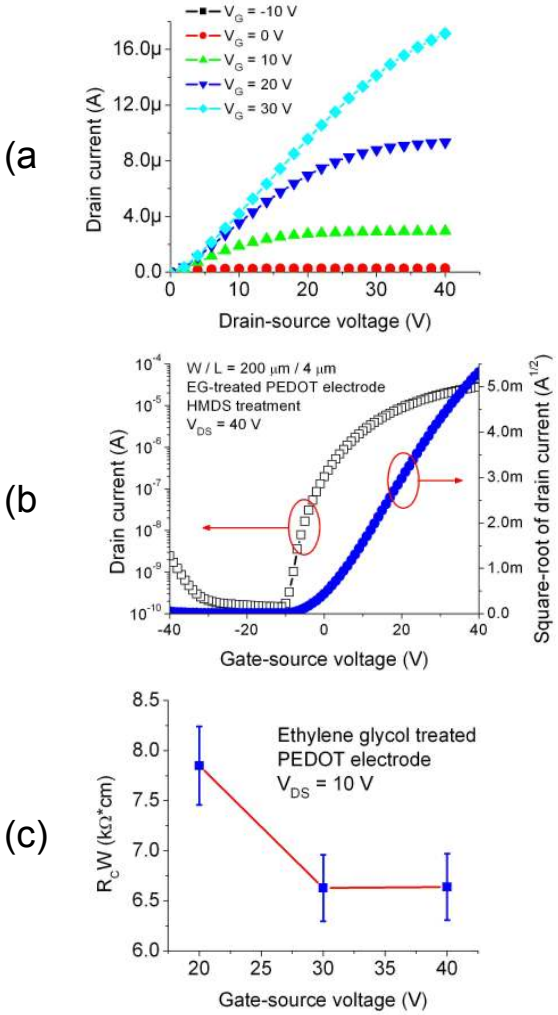


Fig. 3.8 Characteristics of PDI-8CN_2 OFETs with EG-PEDOT electrodes; (a) output characteristics (b) transfer characteristics of (c) contact resistance with respect to the increased gate voltage

The characteristics of PDI-8CN_2 transistors with EG-treated PEDOT electrodes are shown in Fig. 3.8. The saturation regime mobility is increased obtained to 2.3 x 10^{-2} cm^2/Vs and this mobility is comparable to the mobility obtained using Au electrodes. Linear mobility is further increased up to 1.3 x 10^{-2} cm^2/Vs and contact resistance at 30 V gate voltage is also reduced to a value of only 6.6 KΩ·cm. These results indicated that EG-treated PEDOT electrodes result in superior characteristics of PDI-8CN_2 OFETs. The contact resistances and linear regime mobility with respect to different types of electrodes were compared in the PDI-8CN_2 OFETs and are shown in Fig. 3.9. It clearly shows that employing the conducting polymer by coating on the metal electrodes or using conducting polymer electrodes itself enables to improve the device performance.

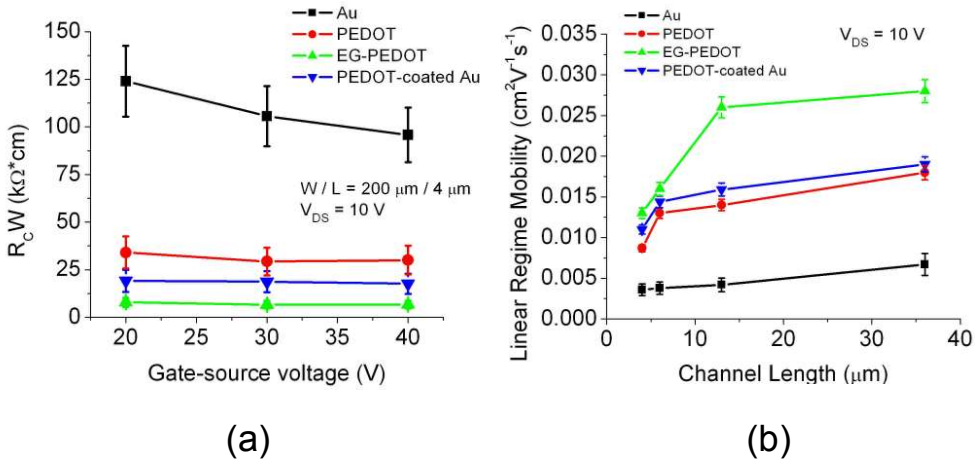


Fig. 3.9 The comparison of (a) contact resistances and (b) linear regime mobility with respect to different types of electrodes in the PDI-8CN_2 OFETs

The microscopic images of untreated PEDOT/PSS electrodes and EG-treated PEDOT/PSS electrodes are shown in Fig. 3.10. The electrode edges of EG-treated PEDOT/PSS electrodes were not damaged during lift-off process due to the stronger interchain interaction in the EG-PEDOT with respect to untreated PEDOT. Therefore, the reproducibility and the efficiency of device fabrication can be enhanced for especially small dimension of devices. This result suggests an evidence of increased interchain interaction among the PEDOT chains.

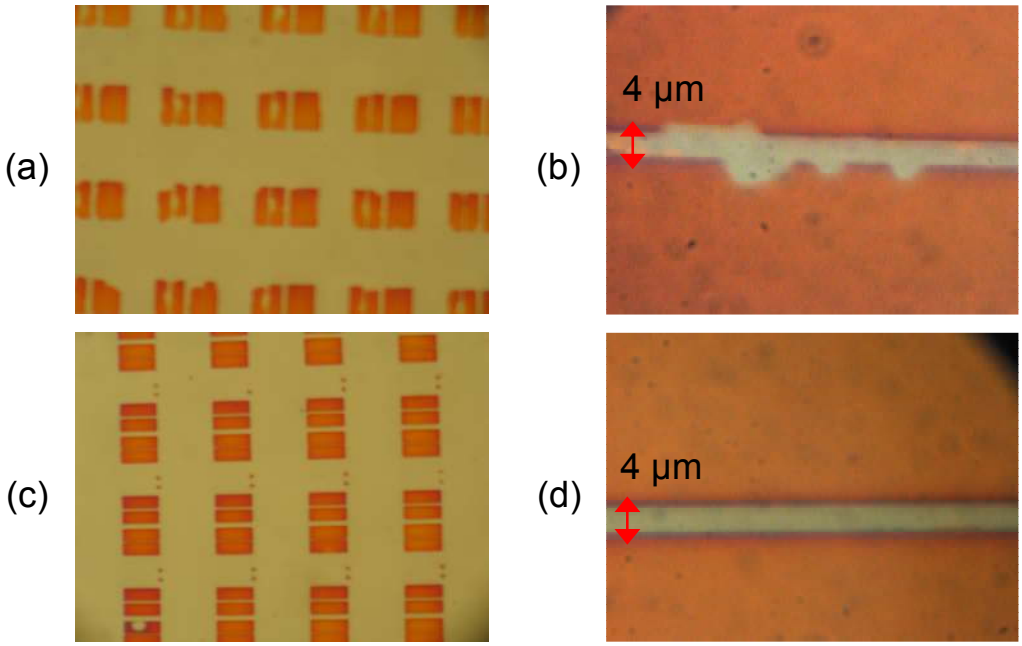


Fig. 3.10 Microscopic top-view images of PEDOT/PSS electrodes at 4 μm channel length FETs; (a) untreated PEDOT/PSS electrodes (b) magnification of untreated PEDOT/PSS electrodes. (c) EG-treated PEDOT/PSS electrodes (d) magnification of EG-treated PEDOT/PSS electrodes. The channel length is 4 μm

3.3 Poly(4-vinylphenol) as the gate dielectric

The role of the gate dielectric is one of the most important factors in OTFTs. SiO_2 has been widely used in both inorganic and organic semiconductor FETs due to its stability and excellent leakage characteristics. However, polymeric dielectrics are better suited for flexible device applications. Spin coating is usually performed to make the gate dielectric with polymers followed by curing at an elevated temperature to cross-link the molecules in the polymer. One of the most common polymeric dielectrics is poly(4-vinylphenol) (PVP) because it forms a smooth thin film with methylated poly(melamine-co-formaldehyde) as a cross-linker [103,107,108]. It can be easily etched by oxygen plasma for further processing. However, it has pores inside the dielectric film despite the fact that methylated poly(melamine-co-formaldehyde) enables the formation of a cross-linked film with PVP. These pores may act as impurities and the amount and size of these pores depends on the degree of linking in the process. The chemical structures of PVP, poly(melamine-co-formaldehyde), and propylene glycol methyl ether acetate (PGMEA) as a solvent are shown in Fig. 3.11.

Fig. 3.12 presents the structure of bottom contact PDI-$8CN_2$ FETs with PVP dielectric. Nickel (Ni) was chosen as the common gate for implementing an organic complementary inverter. The organic complementary inverter with PVP as a gate dielectric will be discussed in the next chapter. Ni was deposited on the Si/SiO_2 substrates by e-beam evaporation. For the gate dielectric layer, PVP solution was prepared. All the materials were purchased from Sigma-

Aldrich. PVP and methylated poly(melamine-co-formaldehyde) as a cross-linker were mixed in PGMEA. The concentration of PVP is ~ 7 wt% of PGMEA and that of cross-linker is ~ 60 wt% of PVP. The cross-linker increases the chemical resistivity of the dielectric with respect to the organic solvents by connecting PVP molecules. It also assists to reduce the porosity of the dielectric and impedes swelling of the PVP dielectric. The solutions were prepared in a nitrogen hood and stirred overnight before use. PVP solution was deposited by spin coating on top of Ni under nitrogen ambient. The spin speed and time was 4000 rpm for 1 min. The samples were then cured at ~180 °C for 1.5 hours in nitrogen ambient. The electrodes were patterned by conventional photolithography and 2.5nm of Ti and 35nm of Au was deposited by e-beam evaporation. Finally, 35 nm of PDI-8CN_2 was thermally evaporated at a substrate temperature of 100 °C to enhance grain growth. The growth rate of the semiconductor was 0.2-0.6 Å/s. The channel lengths of the devices were 4 μm and 12 μm. The channel widths of devices were 200 μm. Measurements were conducted with an Agilent 4155C semiconductor parameter analyzer and the HP 4284A LCR meter to measure the capacitance. All devices are measured at a base vacuum of ~ $2x10^{-3}$ Torr.

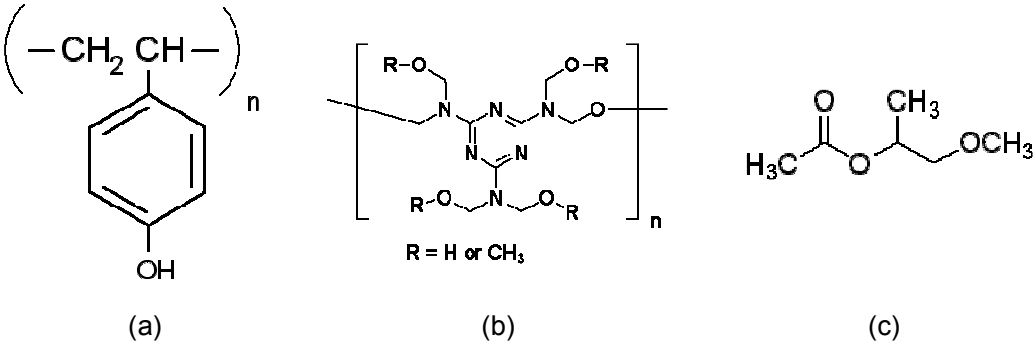


Fig. 3.11 The chemical structures of (a) poly(4-vinylphenol) (PVP) (b) poly(melamine-co-formaldehyde) (c) propylene glycol methyl ether acetate (PGMEA)

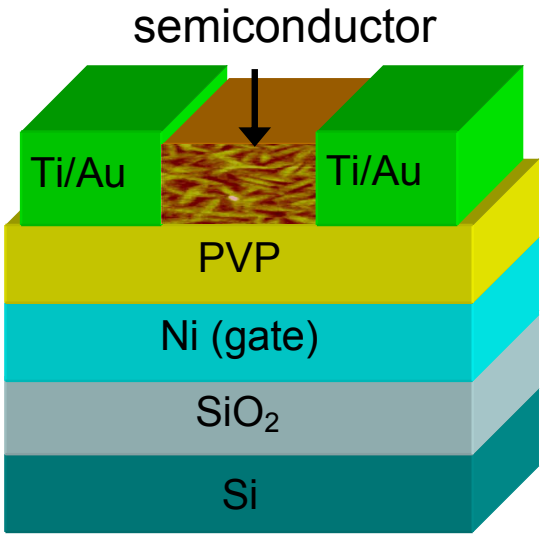


Fig. 3.12 The schematic representation of PDI-8CN_2 devices with PVP dielectric

Fig. 3.13 shows the transfer and output characteristics of PDI-8CN_2 OFETs with PVP dielectric. Measured capacitance of PVP dielectric was 22 nF/cm^2. Noticeable hysteresis was not found for both 4 μm and 12 μm devices and high off currents were observed in both devices. Leakage currents of both

devices were relatively high with respect to the devices with SiO_2 dielectric and the level was several tens of nano-amperes. The saturation regime mobilities of both devices were approximately one of order magnitude lower than that of devices with SiO_2 dielectric.

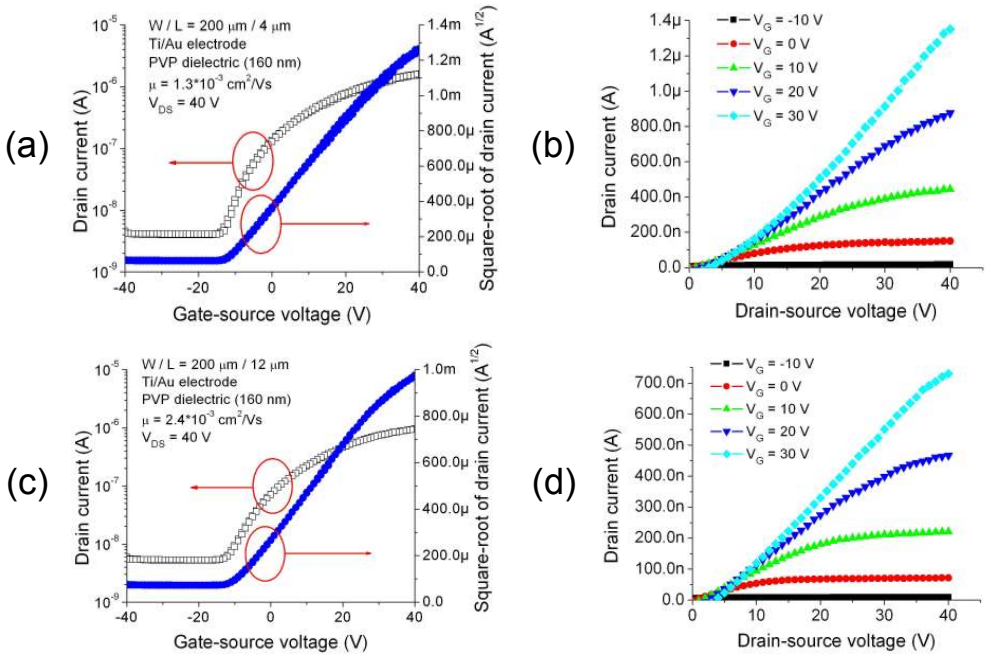


Fig. 3.13 The transfer and output characteristics of PDI-$8CN_2$ OFETs with PVP dielectric. (a) I_{DS} versus V_G at L= 4 μm devices, calculated saturation regime mobility = 1.3 X 10^{-3} cm^2/Vs (b) I_{DS} versus V_{DS} at L= 4 μm devices (c) I_{DS} versus V_G at L= 12 μm devices, calculated saturation regime mobility = 2.4 X 10^{-3} cm^2/Vs (d) I_{DS} versus V_{DS} at L= 12 μm devices. The gate bias was swept from negative to positive voltage

3.4 Conclusion

The improvements in device performance such as field-effect mobility and contact resistance were evaluated with PEDOT/PSS electrodes in PDI-8CN_2 OFETs. We investigated a new technique which is direct coating of PEDOT/PSS solution on the metal electrodes using the hydrophilic properties of PEDOT/PSS solution. It may affect the injection barrier and morphology at the interface between the electrodes and the semiconductor layer. As a result, it showed that both saturation and linear regime mobility were increased with respect to that of the devices that used only PEDOT/PSS electrodes. The contact resistance was reduced by almost 100-folds in comparison with the devices that used Au electrodes. For the low cost fabrication of OTFT on flexible substrates, conducting polymers need to be solely used and the electrical properties of devices with PEDOT/PSS electrodes have generally been inferior due to their relatively low conductivity. Conductivity enhancement of PEDOT/PSS by adding EG was reported [100,101], and we exploited this effect to fabricate OFETs. Immersing the samples with PEDOT/PSS electrodes in EG was chosen instead of adding EG for ease of fabrication. The mobility was similar to that of the devices using PEDOT/PSS coated Au electrodes and the contact resistance was further reduced to 6.6 KΩ·cm. Additionally, EG treatment on PEDOT/PSS electrodes gives rise to the rigid electrode pattern without the delamination of the edges of the electrodes during lift-off. It results from the stronger interchain interaction in the EG-PEDOT, so that the fabrication reproducibility can be especially improved for devices which have small dimensions. Bottom-contact

PDI-8CN_2 OFETs with PVP as the polymer dielectric were also demonstrated. The transfer characteristics of devices showed no noticeable hysteresis. However, high off currents were measured in both devices and leakage currents were relatively high with respect to the devices with SiO_2 dielectric.

CHAPTER 4 ORGANIC COMPLEMENTARY CIRCUITS

4.1 Introduction

Organic field-effect transistors (OFETs) have significant potential for use in a wide range of inexpensive and high volume applications such as radio-frequency identification tags, electronic paper, display driving electronics, and sensors [19-27]. The development of organic transistor-based circuits has been limited to p-channel organic circuits, because of the paucity of environmentally robust high-performance n-channel organic semiconductors [109-111]. Recent literature summary of high speed p-channel or n-channel organic circuits is shown in Table 4.1. The lack of appropriate n-type materials is primarily due to the instability of the n-type charge carriers in most organic semiconductors, particularly upon exposure to moisture or oxygen. Hence, the discovery and implementation of environmentally stable high-mobility n-channel organic transistors has been crucial for the fabrication of fast and reliable organic complementary metal-oxide-semiconductor (CMOS) circuits. Combining p-channel and n-channel transistors enables the fabrication of complementary circuits which exhibit lower power dissipation, greater speed, and better noise margins [21,71,111,112]. Several studies have been reported for high speed complementary organic logic circuits and the recent results are summarized in Table 4.2.

Compound	Type	Circuit	L (μm)	Speed (kHz)	Refs
P3HT	PMOS	Ring oscillator	2.6	192	113
N/A	PMOS	Shift register	4	5	109
Regioregular poly(3-alkylthiophene)	PMOS	Ring oscillator	2	106	114
Pentacene	PMOS	Ring oscillator	10	1.7	111
Fullerene (C60)	NMOS	Ring oscillator	2.5	30.4	115
Methanofullerene [6,6]-phenyl-C71-butyric acid methyl ester ([70]PCBM)	NMOS	Ring oscillator	1.5	2.1	116

Table 4.1 Literature summary of the speed of non-complementary organic logic circuits (except the inverter)

Compound		Circuit	L (μm)	Speed (kHz)	Refs
P-type	N-type				
Nickel dithiophene	Nickel dithiophene	Ring oscillator	5	0.71	117
Pentacene	Hexadecafluorocopperphthalocyanine ($F_{16}CuPc$)	Ring oscillator	2	12.5	118
Dihexyl-α-quinquethiophene (DH-α5T)	Hexadecafluorocopperphthalocyanine ($F_{16}CuPc$)	Ring oscillator	7.5	10	71
α-sexithiophene (α-6T)	Hexadecafluorocopperphthalocyanine ($F_{16}CuPc$)	D-flip flop	7.5	1	71

Table 4.2 Literature summary of the speed of complementary organic logic circuits (except the inverter)

In this chapter, the fabrication and testing of several kinds of complementary organic circuits such as inverter, ring oscillator, and D flip-flop are discussed. Pentacene is commercially available from Sigma Aldrich and it is chosen as the p-type semiconductor due to its high mobility and ease of use. We have shown a number of promising candidates for high-mobility n-type semiconductors such as DFHCO-4T and PDI-8CN_2 in the previous chapter. The fabrication procedures and the electrical characteristics of complementary circuits fabricated with these materials are comprehensively addressed.

4.2 Inverter

4.2.1 TOP-CONTACT INVERTER

Top-contact OFETs generally exhibit a better performance in comparison with bottom-contact devices. Since the characteristics of DFHCO-4T transistors were encouraging, we fabricated a top contact complementary inverter. An inverter is a device for converting direct current into alternating current. It utilizes two types of MOSFETs, a n-channel FET and a p-channel FET. The input is given to the gate terminals of both FETs. The drains of the both FETs are connected together and form the output terminal. The supply voltage is connected to the source of the p-channel FET as V_{DD}, and the source of n-channel FET is grounded. When the input voltage is zero, the p-channel FET turns on, and the n-channel FET turns off. Alternatively, the p-channel FET is off and the n-channel FET is on when the applied input voltage is high. Both the devices are connected in series, so that the drain current is ideally zero except during the switching operation. Only a small charging current flows during the switching operation, so that the power dissipation is small in comparison with a PMOS inverter. The schematic of the complementary inverter is shown in Fig. 4.1(a).

The circuit was fabricated on HMDS-treated Si/SiO_2 substrates. A heavily doped Si substrate was used as the gate with 100 nm of thermally grown SiO_2. 40 nm of pentacene was sublimed by shadow masking the p-channel region and DFHCO-4T was sublimed to a similar thickness over the n-type region with the substrate temperature maintained at 60 ºC to enhance grain growth. 45 nm of gold was evaporated using a shadow mask over the structure to form the

source and drain electrodes. The channel widths and lengths are 3.8 mm and 1.8 mm, respectively. The device structure of the top-contact complementary inverter is shown in Fig. 4.1(b).

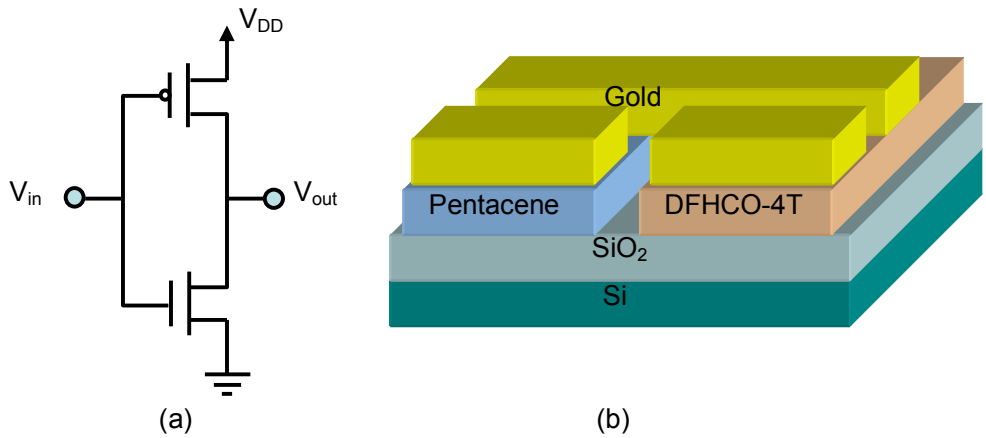
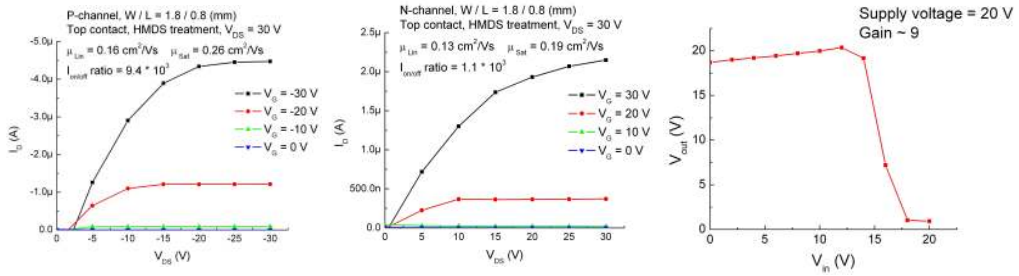


Fig. 4.1 (a) schematic representation of the complementary inverter (b) device structure of the top-contact complementary inverter. Pentacene and DFHCO-4T were used as p-type and n-type semiconductor, respectively. Heavily doped Si that served as the common gate was used as the input and it is connected to the both FETs. The drains of the both FETs are connected together and form the output terminal

Fig. 4.2(a) and (b) show characteristics of the p-channel and n-channel transistors, respectively and each device shows good output characteristics. The resulting voltage transfer characteristic of the complementary inverter is shown in Fig. 4.2(c). This transfer characteristic shows good inverter characteristics and measured gain is approximately 9. This result demonstrated that DFHCO-4T and pentacene can be processed on a common dielectric, with similar common surface treatment, and the same electrode metal type in the top contact configuration. However, the bottom-contact configuration is favorable for

practical electronics requiring shorter channel lengths (< 10 μm) and the saturation mobility of bottom contact transistor with DFHCO-4T is more than one order of magnitude lower than that of its top contact counterpart. In addition, DFHCO-4T is not an air-stable material. Therefore, we employed another n-type material, PDI-8CN_2 for the bottom-contact complementary inverter.



(a) (b) (c)

Fig. 4.2 (a) output characteristics of 0.8 mm channel length (W / L = 2.25) top contact pentacene FETs with HMDS treatment in vacuum (b) output characteristics of 0.8 mm channel length (W / L = 2.25) top contact DFHCO-4T FETs with HMDS treatment in vacuum (c) voltage transfer characteristics of the complementary inverter in vacuum. Supplying voltage is 20 V

4.2.2 BOTTOM-CONTACT INVERTER

PVP was the gate dielectric used in all organic circuits starting with the bottom-contact complementary inverter. Metal-insulator-metal capacitors were fabricated on PVP to determine the conditions under which the devices could survive the appropriate electric field. Fig. 4.3(a) presents the structure of a capacitor with PVP dielectric. After Ni was deposited on the Si/SiO_2 substrates

by e-beam evaporation, PVP solution was spin-coated on top of Ni under nitrogen ambient. The samples were cured at ~180 °C for 1.5 hours in nitrogen. The final step was the e-beam evaporation of a metal cap which consisted of 2.5nm of Ti and 35nm of Au. The width and length of metal cap were 200 μm and 70 μm, respectively.

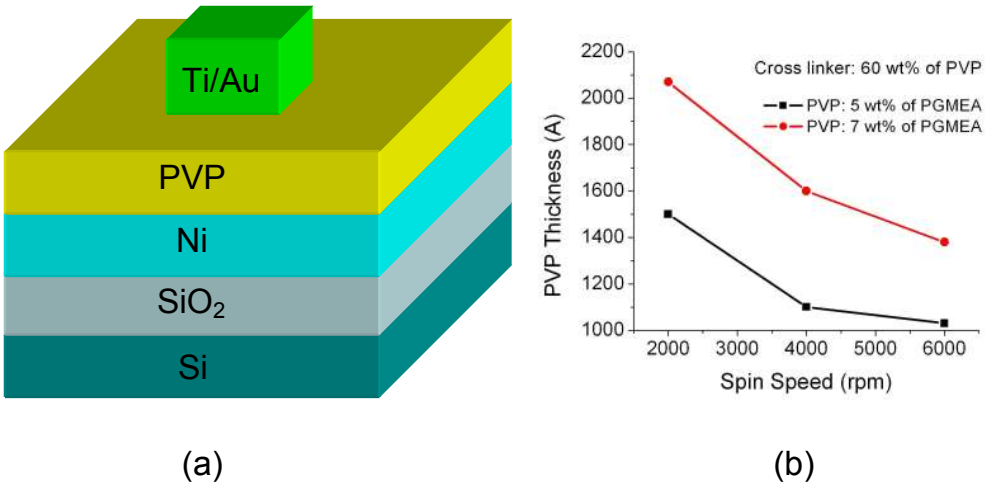


Fig. 4.3 (a) the capacitor structure with Ni as the gate and PVP as the gate dielectric (b) PVP thickness versus spin speed of the PVP solution. Thickness of the PVP dielectric decreases with increasing the spin speed.

The PVP thickness variation as a function of spin speed is shown in Fig. 4.3(b). Two levels of PVP concentrations were chosen at ~ 5 and ~ 7 wt% of PGMEA with the concentration of the cross-linker kept constant at ~ 60 wt% of PVP. The spin speed was changed from 2000 rpm to 6000 rpm. As a result, the dielectric thickness decreased with increasing the spin speed. Thinner dielectric is favorable for low-voltage applications. However, leakage current is an important concern before the application of the polymer dielectric. With

these samples, the leakage current density as a function of electric fields with respect to different concentrations of PVP solution and spin speed was observed as shown Fig 4.4. The leakage current increased as the concentration of PVP went down and as the spin speed increased. When the concentration of PVP is ~ 7 wt% of PGMEA and the spin speed is 2000 rpm, the magnitude of leakage current of the capacitor is below a micro-ampere for a voltage range of -40 V to 40 V. Accordingly, this condition was employed to fabricate organic complementary circuits with PVP dielectric.

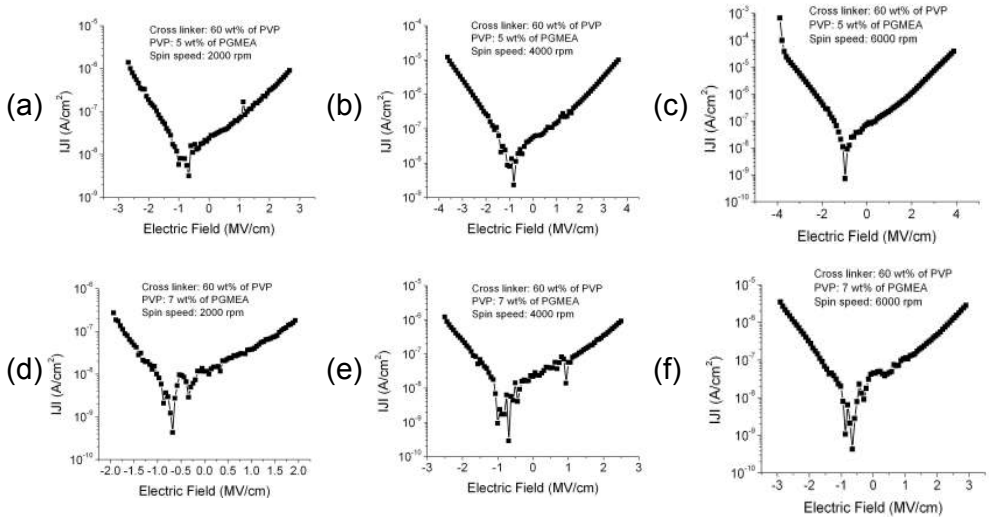


Fig. 4.4 Leakage current density as a function of electric fields with respect to different concentrations of PVP solution and spin speeds. The concentration of cross-linker was kept constant at ~ 60 wt% of PVP; (a) the concentration of PVP is ~ 5 wt% of PGMEA and the spin speed is 2000 rpm (b) the concentration of PVP is ~ 5 wt% of PGMEA and the spin speed is 4000 rpm (c) the concentration of PVP is ~ 5 wt% of PGMEA and the spin speed is 6000 rpm (d) the concentration of PVP is ~ 7 wt% of PGMEA and the spin speed is 2000 rpm (e) the concentration of PVP is ~ 7 wt% of PGMEA and the spin speed is 4000 rpm (f) the concentration of PVP is ~ 7 wt% of PGMEA and the spin speed is 6000 rpm

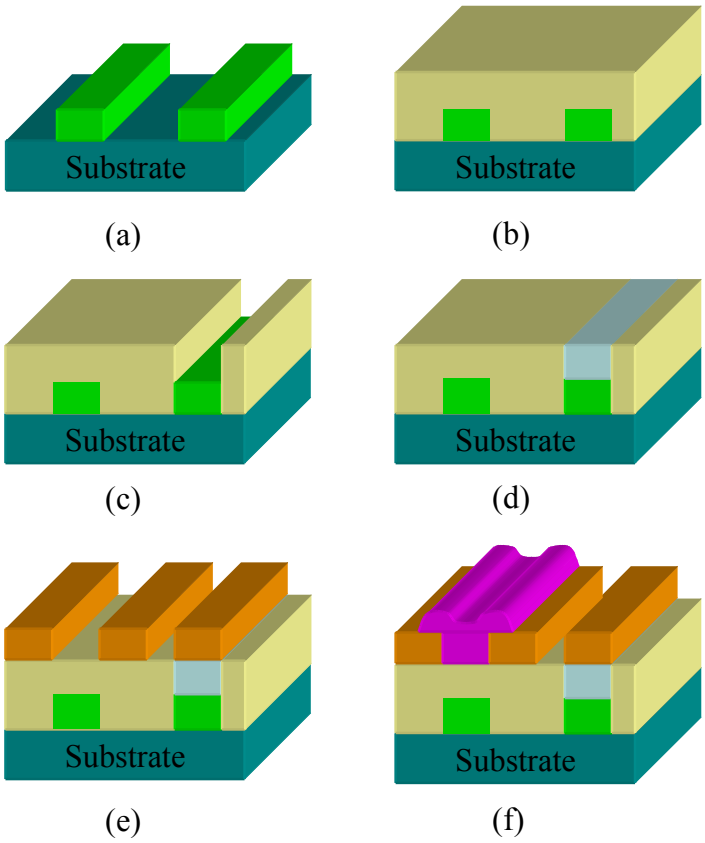


Fig. 4.5 The fabrication procedure for bottom-contact complementary inverter with PVP dielectric. Pentacene and PDI-8CN_2 are used as the p-type and n-type semiconductor, respectively. The gate is patterned and there are three variations in device dimension; W / L = 20000 / 10 μm, 10000 / 5 μm, 1000 / 3 μm; (a) gate metal (Ni) deposition (b) PVP layer by spin coating (c) gate via opening (d) contact metal deposition (e) source and drain electrodes (Ti/Au) deposition (f) the deposition of pentacene and PDI-8CN_2

The fabrication procedure for complementary circuits with PVP dielectric is demonstrated in Fig. 4.5. SiO_2 on top of silicon formed the substrates. The gate was patterned by conventional lithography and Ni was deposited by e-beam evaporation. The samples were cleaned by oxygen plasma. PVP solution was

then deposited by spin coating and cured at ~180 °C for 1.5 hours in nitrogen ambient. After the photoresist was developed for the via, oxygen plasma was performed to open the via. Chromium was evaporated to fill the via and 2.2nm of Ti and 35nm of Au were deposited by the e-beam evaporation. 40 nm of PDI-8CN_2 was thermally evaporated by shadow masking of n-channel region with the substrate temperature held at 100 ºC and same thickness of pentacene was sublimed over the p-type region with the substrate temperature kept constant at 60 ºC to enhance grain growth. Discrete inverters have three different channel lengths which are 10 µm (W / L = 2000), 5 µm (W / L = 2000), and 3 µm (W / L = 333). The device dimensions of the n-channel FET and the p-channel FET in a given inverter were constant. Measurements were conducted with an Agilent 4155C semiconductor parameter analyzer at a vacuum probe station with a base pressure of ~ 2 mTorr.

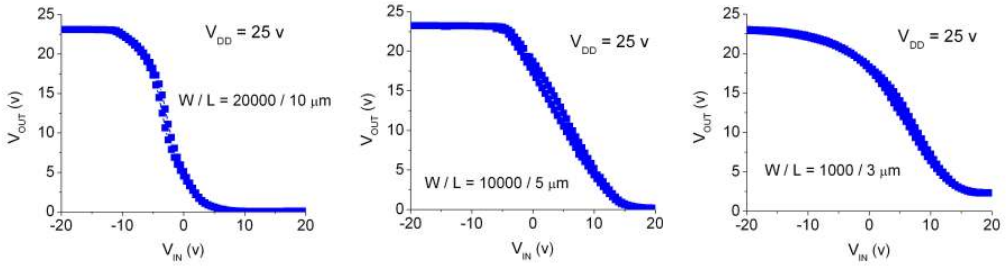


Fig. 4.6 Voltage transfer characteristics of the complementary inverter in vacuum for (a) W / L = 20000 / 10 µm (b) 10000 / 5 µm (c) 1000 / 3 µm. Supply voltage is 25 V. The input voltage was swept from negative to positive voltage

Fig. 4.6 shows the voltage transfer characteristics of the complementary inverter with different channel lengths. The V_{DD} was set to 25 V and the input voltage was swept from -20 V to 20 V and back to -20 V to examine any hysteresis. No noticeable hysteresis was found in any of the inverters with variable channel lengths. When the input voltage is low, the output voltage is slightly less than V_{DD} because a certain amount of off-current flows into the n-channel FET. These transfer characteristics reflect reasonable characteristics for a complementary inverter. However, the measured gain is not high in comparison with an inorganic complementary inverter, W/L ratios of each transistor being the same. However, the saturation mobility of pentacene is higher than that of PDI-8CN_2 on a PVP dielectric, necessitating the W/L ratios of the n-channel FETs to be larger than that of the p-channel FET for optimization of the performance of the complementary inverter. The large negative threshold voltage of n-channel FETs results in the negative shift of the transition region. Relatively large off-currents were found in PDI-8CN_2 devices with PVP dielectric. This is a critical problem that affects the performance of circuits and contributes to threshold voltage instability. Therefore, organic complementary ring oscillators were implemented using a bilayered structure with inorganic dielectrics. This is discussed in the next section.

4.3 Ring oscillator

The maximum switching frequency of a single transistor is a function of the mobility, terminal voltages, and channel length as well as parasitic and overlap capacitances. A ring oscillator is formed by connecting an odd number of inverters in a loop and it is often used in clock generation circuits. Each inverter triggers the next inverter in a cascade connection, and the last inverter triggers the first. Therefore, the oscillation is sustained because the number of inverters is odd. The schematic of a five-stage ring oscillator is shown in Fig. 4.7(a). The operating frequency of the ring oscillator is an indicator of the maximum speed at which digital circuits can be implemented. The maximum oscillation frequency and propagation delay reported are 12.5 kHz and 8 μs, respectively [118].

We fabricated complementary five-stage ring oscillators with PDI-8CN2 as the n-channel material and pentacene as the p-channel material due to high mobilities achieved in bottom-contact transistors made from these materials. Fig. 4.7(b) shows the structure of discrete FETs. The bottom-contact structures of the discrete OFETs are fabricated on silicon substrates with aluminum interconnect metal and double gate dielectric layers, consisting of 200 nm of silicon nitride and 100 nm of silicon oxide. These were fabricated in a similar fashion as has been previously reported [71]. The channel width and channel length of the individual transistors are 2.0 mm and 7.5 μm, respectively. Both HMDS and 1-hexadecanethiol (HDT) treatment were performed. For the HDT treatment, the samples were kept in HDT vapor for 20 min at 135 °C in nitrogen

ambient and cleaned with ethanol. The deposition conditions of the PDI-8CN2 film were the same as those used in the fabrication of discrete transistors. Pentacene is purified by sublimation and 42 nm of the purified pentacene was evaporated at 60 °C. All electrical characterizations was carried out under vacuum (~1 mTorr) at 300 K with an Agilent 4155C semiconductor parameter analyzer. An Oscilloscope (LeCroy 6030) was used to evaluate the output characteristics of the ring oscillator. A diagram of the measurement setup is illustrated in Fig. 4.8.

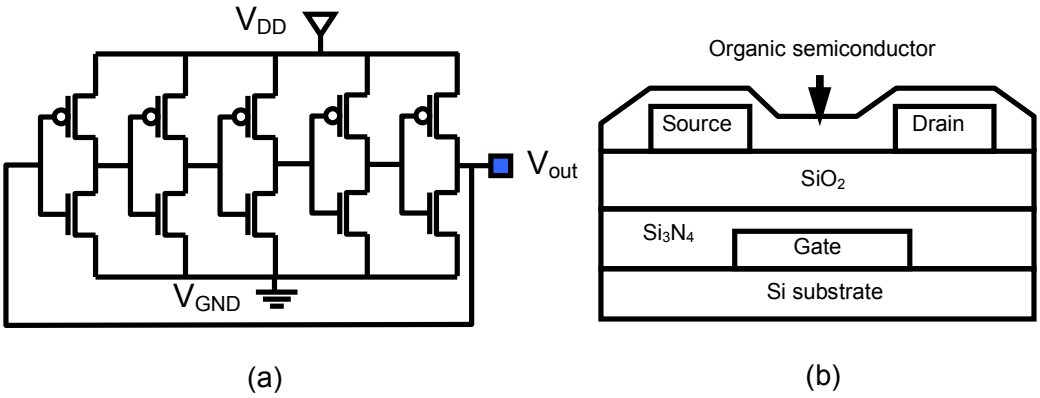


Fig. 4.7 (a) Schematic of a five-stage complementary ring oscillator without buffer stage (b) the structure of a bottom-contact OFET device

Fig. 4.9 shows the oscillation frequency characteristics with a supplying voltage of 100 V and a channel length of 7.5 μm. An oscillation frequency of 34 kHz was achieved with a propagation delay (t_p) per stage of ~3 μs. In general, the ring oscillator with a certain odd number of inverters (N) will oscillate with the period of $2Nt_p$. Although a higher oscillation frequency was recently reported for a PMOS configuration with shorter channel lengths [113], to our knowledge, the present result is the highest oscillation frequency reported for an

organic CMOS configuration [71,118]. The improved performance of this device is due to the significant improvement in the n-channel mobility; however, the mobility of carrier in the n-channel is still somewhat lower than that of the p-channel. The ring oscillator frequency can be improved by increasing the mobility of n-channel materials further as well as by reducing channel lengths and overlap capacitances between the source/drain electrodes and the gate.

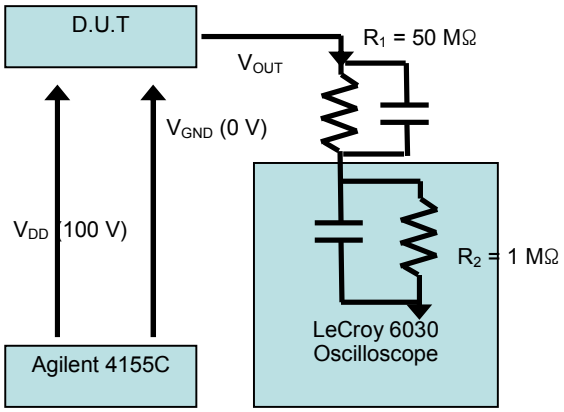


Fig. 4.8 Experimental setup for ring oscillator measurement (D.U.T = device under test)

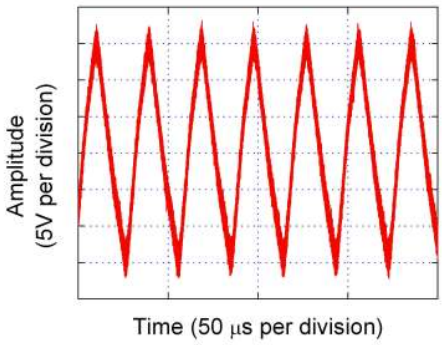


Fig. 4.9 Oscillation of 34 kHz in a five stage ring oscillator with V_{supply} = 100 V. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 88, 082104 (2006). Copyright 2006, American Institute of Physics

4.4 D flip-flop

Organic complementary metal-oxide-semiconductor (CMOS) clocked circuits based on organic transistors have been reported [118]. However, the maximum clock rate is only 1 kHz [71]. We demonstrated that the implementation of PDI-8CN_2 and the effect of electrode/dielectric surface treatment had a great potential for high speed organic complementary circuits. Therefore, an organic semiconductor-based complementary D flip-flop with PDI-8CN_2 and pentacene was fabricated and characterized.

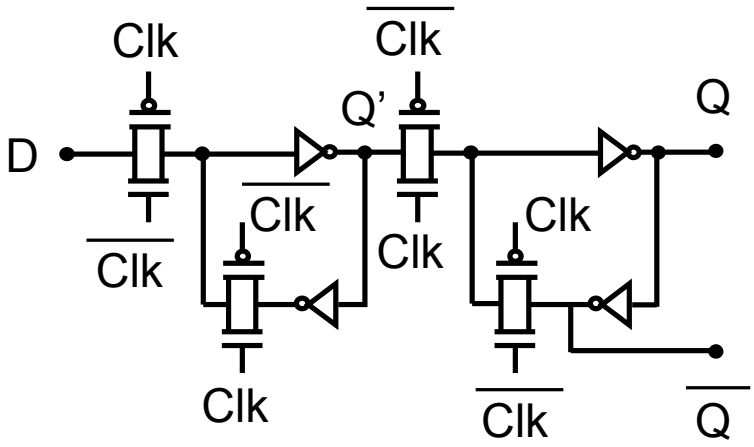


Fig. 4.10 Schematic diagram of a conventional D flip-flop

The D flip-flop is a basic storage element to construct sequential logic circuits and systems. A conventional master-slave D flip-flop schematic diagram is illustrated in Fig. 4.10. The pass-transistor logic based D flip-flop requires 16 transistors which is less than the transistors required for NOR/NAND

based logic. The D flip-flop is usually composed of two latches and each latch consists of two CMOS transmission gates and two inverters. When the clock (Clk) is low, the input data D passes directly to the node Q'. Since the clock bar is high at the same time, node Q' is separated from the output node Q, and the feedback loop is closed so that the slave latch is in the storage state. The input data are sent to the slave latch when the clock is high. Therefore, the output starts to collect at the node Q when the input data D is at logic 1 and the clock converts from logic 0 to 1.

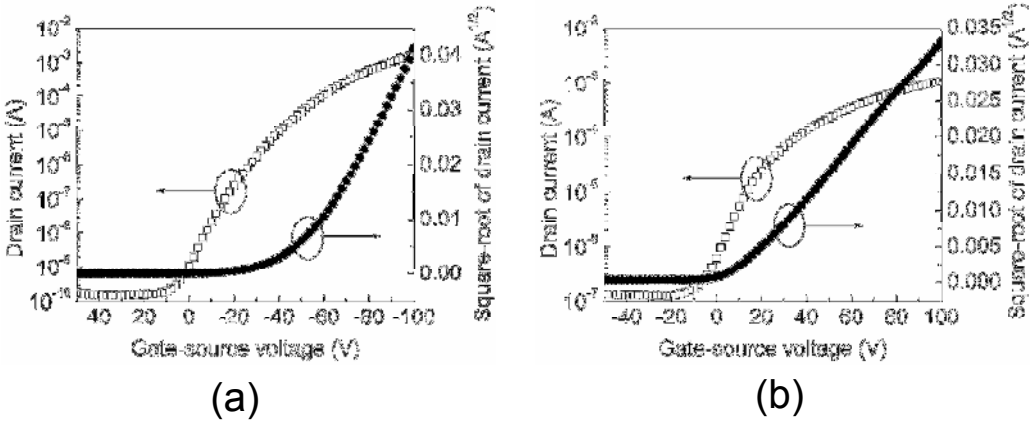


Fig. 4.11 Transfer characteristics of (a) pentacene OFETs and (b) PDI-8CN_2 OFETs. W / L = 2000 / 7.5 μm. The devices are measured in air. Reprinted with permission from Byungwook Yoo, *et. al.*, IEEE Elect. Dev. Lett. 27, 737 (2006). Copyright 2006, IEEE

The bottom-contact structures of the discrete OFETs were the same as those in the previous section as shown in Fig. 4.7(b). The channel channel length and width of the individual transistors are 2.0 mm and 7.5 μm, respectively. The use of SAMs in organic devices passivates the hydrophilic

inorganic substrate with a lower surface energy monolayer [39,43]. In addition, alkanethiols were used to modify the surface energy of the gold electrodes to facilitate charge carrier injection. Thus, prior to the semiconductor deposition, samples were treated with HMDS vapor to functionalize the oxide-based substrate/dielectric, followed by HDT vapor to functionalize the gold electrodes. The PDI-8CN_2 was purified by multiple recrystallizations and thermally deposited onto the substrate maintained at 100 °C to a thickness of 42 nm. Pentacene films (42 nm) were deposited on the discrete FETs at a substrate temperature of 60 °C. The base pressure was 4×10^{-7} Torr and the deposition rate was 0.2-0.7 Å/s for these depositions. All electrical characterization was conducted in ambient atmosphere at room temperature. In the case of the complementary organic D flip-flops, the surface treatments and the deposition conditions used were the same as those used in the fabrication of the discrete transistors. The transfer characteristics of discrete bottom-contact pentacene and PDI-8CN_2 transistors, treated with both HMDS and HDT, are shown in Fig. 4.11. For PDI-8CN_2 transistors, the field effect mobility calculated in the saturation regime was $6.3x10^{-2}$ cm^2/Vs at a source-drain voltage of 100 V where I_{on}/I_{off} ratio (V_{DS} = 100 V) was $8.7x10^3$ and threshold voltage was 9.8 V. Most n-channel OFETs exhibit degradation in electrical properties in ambient atmosphere; however, the mobility of PDI-8CN_2 in the saturation regime is comparable to the mobility obtained in vacuum, as shown in Fig 2.14. For pentacene transistors, the field effect mobility calculated in the saturation regime was 0.29 cm^2/Vs at a source-drain voltage of -100 V where I_{on}/I_{off} ratio (V_{DS} = -100 V) was $1.1x10^7$.

A diagram of the measurement setup for D flip-flops is illustrated in Fig. 4.12. 100 V of V_{DD} and 0 V of V_{GND} are supplied from an Agilent 4155C

semiconductor parameter analyzer to the sample. The Tektronix AWG 2005 arbitrary waveform generator creates and supplies the clock and clock bar signal. These signals are amplified to 100 V by the Avtech pulse amplifier and supplied to the sample. The position of this pulse is set at the rising edge of the clock pulse. These input signals are monitored by a LeCroy 6030 oscilloscope. All D flip-flop measurements are in air.

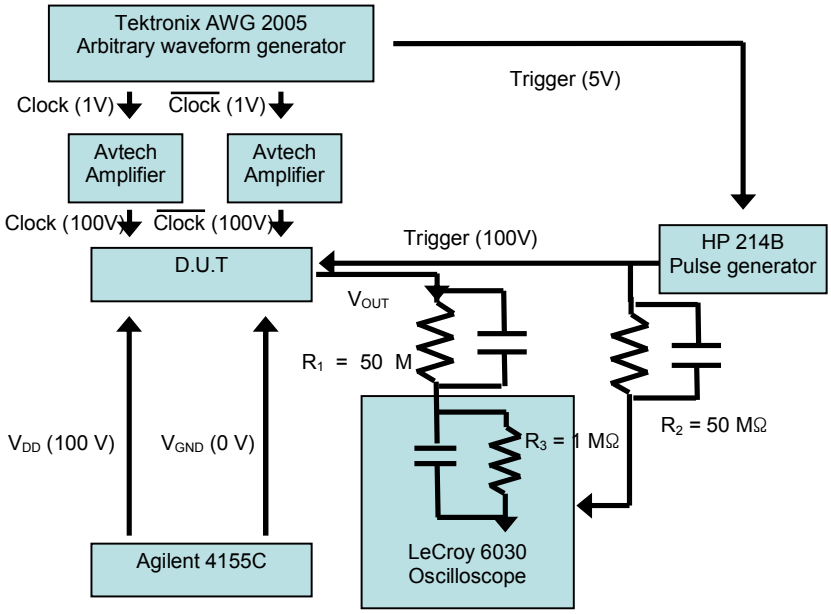


Fig. 4.12 Experimental setup for D flip-flop measurement

The measured and simulated characteristics for a pass transistor logic based D flip-flop at a clock frequency of 1 kHz are shown in Fig. 4.13(a). The black line, blue line, green line, and red line represent the measured output, simulated output, data signal, and clock signal, respectively. All FETs in the D flip-flop have the same dimensions which are 2 mm of channel width and 7.5 μm

of channel length. PDI-8CN_2 and pentacene are used for the n-channel OFETs and the p-channel OFETs, respectively. The speed of this D flip-flop is limited by one transmission gate and one inverter delay after the clock switches from logic 0 to logic 1. The fabricated D flip-flop was simulated using the T-SPICE program, using models and procedures similar to that described in [71]. Fig. 4.13(b) shows the measured and simulated characteristics for the same D flip-flop at a clock frequency of 5 kHz. Measured output starts to degrade; however, it still follows the clock and data signal. It can be seen that the proposed circuit can operate correctly within reasonable error ranges caused by the simplicity of the model. This clock rate is the highest achieved so far for an organic complementary D flip flop.

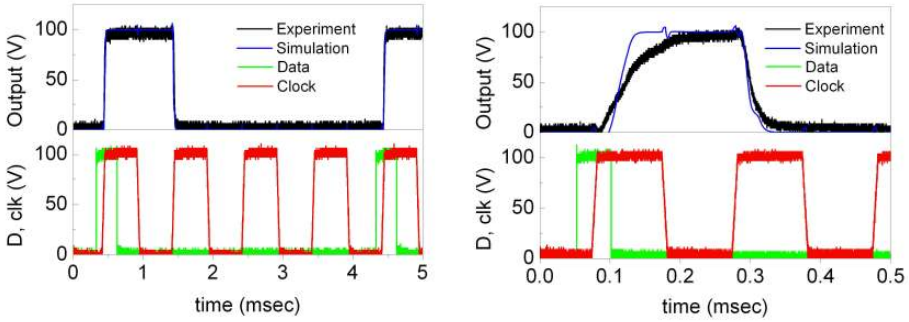


Fig. 4.13 The measured output, simulated output, data signal, and clock signal are illustrated as black line, blue line, green line, and red line, respectively. PDI-8CN_2 and pentacene were used as the n-type and p-type materials, respectively. (a) output characteristics for the organic complementary D flip-flop at (a) 1 kHz and (b) 5 kHz. Reprinted with permission from Byungwook Yoo, *et. al.*, IEEE Elect. Dev. Lett. 27, 737 (2006). Copyright 2006, IEEE

4.5 Conclusion

Top-contact complementary inverters were fabricated with pentacene and DFHCO-4T. It showed good inverter characteristics and the measured gain was approximately 9. For flexible substrates, bottom-contact complementary inverters with PVP as the gate dielectric were fabricated with pentacene and PDI-8CN_2. The voltage transfer characteristics showed reasonable inverter characteristics and no hysteresis was observed. However, a negative shift of the transition region was observed due to the high off-current of PDI-8CN_2 FETs with PVP dielectric. In order to achieve high and stable performance circuits, inorganic dielectric bilayers were used for organic complementary ring oscillators and D flip-flops.

Organic complementary ring oscillators were demonstrated with pentacene and PDI-8CN_2 as the p-type and n-type material, respectively. An oscillation frequency of 34 kHz was obtained in a five-stage ring oscillator operated at a supply voltage of 100 V. Organic complementary D flip-flops with PDI-8CN_2 and pentacene were also fabricated and characterized. We report a clock rate of 5 kHz in air, which is the highest speed that any organic transistor-based complementary clocked circuit has achieved to date. The speed of these complementary circuits will be enhanced by further increasing the mobility of the n-channel FETs as well as by reducing channel lengths and overlap capacitances between the source/drain electrodes and the gate.

CHAPTER 5 SOLUTION-DEPOSITED N-CHANNEL TRANSISTORS AND COMPLEMENTARY CIRCUITS

5.1 Introduction

Printed electronic circuits have been explored for low-cost, large-area applications, such as displays and radio frequency identification tags, where the promise of inexpensive solution-based fabrication techniques is more crucial than the fast circuit speeds associated with conventional inorganic semiconductors [118-122]. In order for such low-cost, portable devices to become a reality, high-mobility, air-stable n-channel OFETs are required to enable the fabrication of organic complementary circuits that would operate at sufficient speeds and with low power dissipation. Additionally, the semiconductors must be solution processible to be compatible with the inexpensive fabrication techniques envisioned for printed electronics. The recent high field-effect mobility values of solution-based n-channel top and bottom contact transistors are summarized in Tables 5.1 and 5.2, respectively.

This solution-based work represents a major advance over the results of Katz *et. al.* in which a simple organic complementary inverter was fabricated with shadow-masked top-contact geometries [34]. Such simple fabrication techniques are not scalable in terms of bringing down the channel lengths to useful levels and also in scaling up the circuit complexity to any circuits other than simple inverters. In the method we demonstrate, circuits of arbitrary

complexity can be fabricated and channel lengths in the technologically useful range (< 10 microns) have been achieved. These last two points represent the crossing of major technical hurdles in the development of organic complementary circuit technology.

Compound	Mobility (cm^2 /Vs)	W / L (μm)	Refs
Methanofullerene 1-(3-methoxycarbonyl)propyl-1-phenyl[6,6]C61	0.025 (with Au) 0.1 (with Ca electrodes)	1000 / 100	125
Poly(9,9-dioctyfluorene)	0.01 (BCB, with Ca electrodes)	N/A	126
Poly(9,9-dioctylfluorene-alt-benzothiadiazole)	0.005 (BCB, with Ca electrodes)	2500 / 25	126
Poly(9,9-dioctylfluorene-alt-bithiophene)	0.006 (BCB, with Ca electrodes)	N/A	126
Poly(2-methoxy-5-(3,7-dimethyloctoxy)-p-phenylene vinylene)	0.002 (BCB, with Ca electrodes)	10^5 / 200	126
C60-fused *N*-methylpyrrolidine-*meta*-C12 phenyl (C60MC12)	0.067 (with Au)	5000 / 20	123
Methanofullerene [6,6]-phenyl C61-butyric acid methyl ester (PCBM)	0.0045 (with Ca electrodes)	7000 / 50	127

Table 5.1 Literature summary of high mobility solution-based n-channel top contact transistors

Compound	Mobility ($cm^2/V s$)	W / L (μ m)	Refs
Nickel dithiolene	Order of 10^{-3}	1000-20000 / 1.5-40	117
Methanofullerene 1-(3-methoxycarbonyl) propyl-1-phenyl[6,6]C61	0.003	1000 / 100	125
Poly(benzobisimidazobenzophenanthroline) (BBL)	0.1	500 / 25	128

Table 5.2 Literature summary of high mobility solution-based n-channel bottom contact transistors

While most examples of printed organic semiconductors are conjugated p-type polymers, solution-processed OFETs with small molecules are far less common [123,124]. In the previous chapter, PDI-8CN_2, a small molecule semiconductor was used to fabricate promising vapor-deposited n-channel OFETs and complementary circuits with excellent electrical performance and remarkable environmental stability. Since PDI-8CN_2 is soluble in common solvents such as chloroform, toluene, and dichlorobenzene, it raises the intriguing question of whether it could be used for fabrication of complex complementary organic circuits using solution-based processing techniques. In this chapter, we report the fabrication of high-performance solution-deposited n-channel organic transistors and complementary circuits using PDI-8CN_2 solution with a micro-injector patterning technique.

5.2 Experimental setup for micro-injection

In contrast to polymers, small molecules cannot be easily processed from solutions. One of the major advantages of PDI-8CN_2 is that despite being a small molecule, it is soluble in standard solvents so that it lends itself well to solution based processing. For the present OFET device fabrication, organic semiconductor solutions were patterned in a nitrogen atmosphere using an Intracel® Picospritzer®, a pneumatically actuated micro-injector. A picture of the Picospritzer® system is shown in Fig. 5.1. The gas pressure and jetting time are controlled by the main body of Picospritzer®. The nitrogen source is connected to the input of the main body and the gas output of the main body is connected to the tip of micropipette. The other end of micropipette is pulled by a Sutter P-2000 laser micropipette puller and the micro-pipette is handled by the manipulator. The motion camera, lens, and light system are installed for function control of the micropipette. A computer is connected to the motion camera to capture videos and images. The temperature controller is set to anneal the samples. The droplet size depends not only on the tip dimension of the micro-pipette but also on the jetting parameters which are jetting distance, jetting time, and gas pressure. The diameter of the micropipette is approximately 20 μm. The jetting parameters were optimized to obtain a reproducible solution droplet.

Solvent selection proved crucial to the formation of uniform semiconductor films. Low-boiling solvents such as chloroform leave residues on the micro-pipette tip, adversely affecting the deposition process and the

resultant film morphology. However, high-boiling point solvents such as 1,2-dichlorobenzene (b.p. 174 ^{o}C) do not adversely affect the solution deposition from the micro-pipette and lead to higher transistor film mobilities. This result is presumably, also a consequence of improved film ordering arising from slower solvent evaporation [129,130].

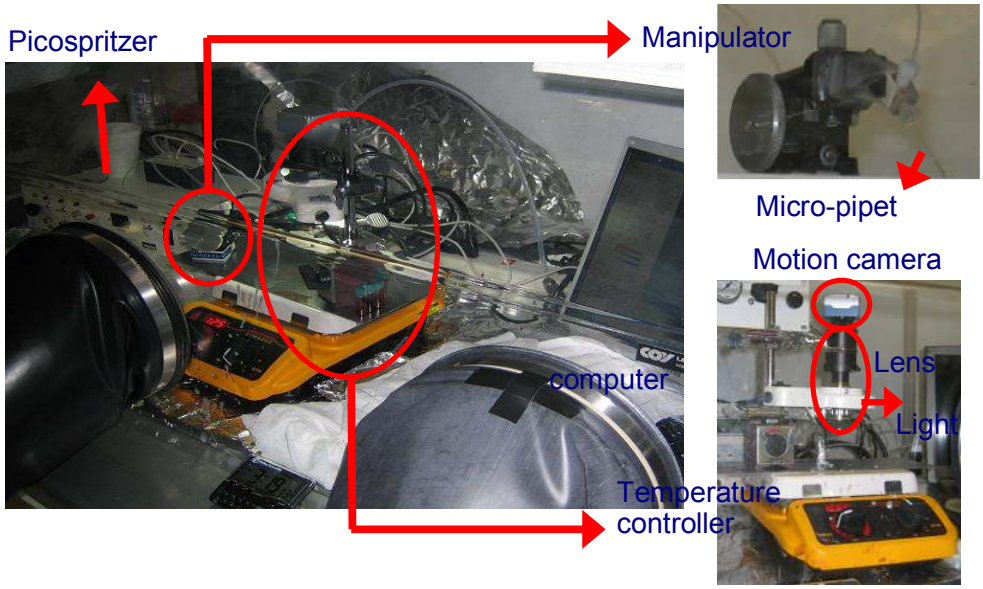


Fig. 5.1 A photograph of the picospritzer system. Nitrogen source tube is connected to the input of picospritzer and output is connected to one end of micro-pipet. A micro-pipet is attached to the manipulator to control the position of solution jetting. The motion camera, lens, light source, and computer are set to catch the trace of micro injecting. A hot plate is under the large metal plate to anneal the samples.

To make smaller sized solution droplet on the samples, dielectric surface treatment was performed and compared. Fig 5.2 shows the microscopic view of jetted PDI-8CN$_2$ droplet on two different samples. One is an oxygen plasma treated sample which is hydrophilic. The other is a HMDS-treated sample which

is hydrophobic. The PDI-8CN_2 solution is more spread out on the hydrophilic surface. The mean diameter of droplets on the hydrophilic surface and the hydrophobic surface are 2.2 mm and 180 μm, respectively. Therefore, in order to produce approximately hemispherical solution droplets, gate dielectric surface treatment must be performed. The droplet size can be further reduced through the reduction in micropipette diameter. Controlling the nature of the solution in terms of its viscosity will also help in reducing droplet diameters.

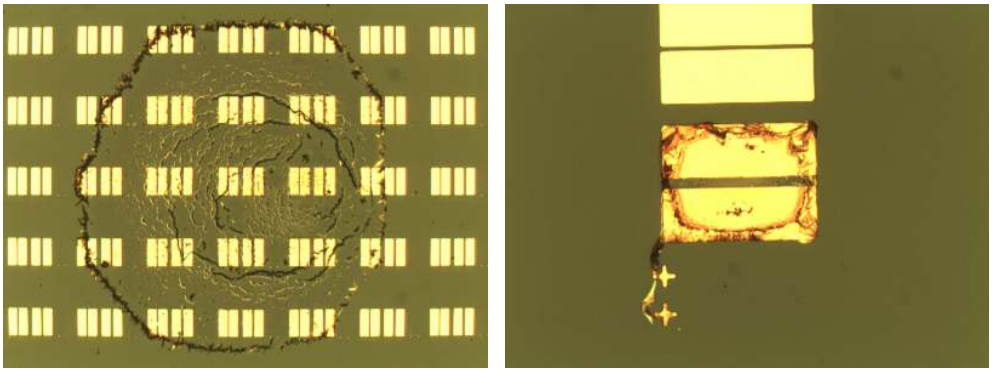


Fig. 5.2 Microscopic view of samples. PDI-8CN2 solution was dropped on (a) the hydrophilic dielectric surface treated by oxygen plasma, and (b) the hydrophobic dielectric surface treated by HMDS. Mean diameter of droplet on the hydrophilic surface and the hydrophobic surface were 2.2 mm and 180 μm, respectively

In order to visualize the crystallization of PDI-8CN2 solution, in-situ video recording was performed as shown in Fig 5.3. The micropipette was positioned by the manipulator for injection of PDI-8CN_2 solution and the solution was injected to the devices in nitrogen ambient. Injected PDI-8CN_2 solution

made hemispherical shapes due to the surface treatment of the gate dielectric and crystallized from the periphery to the center of the droplets.

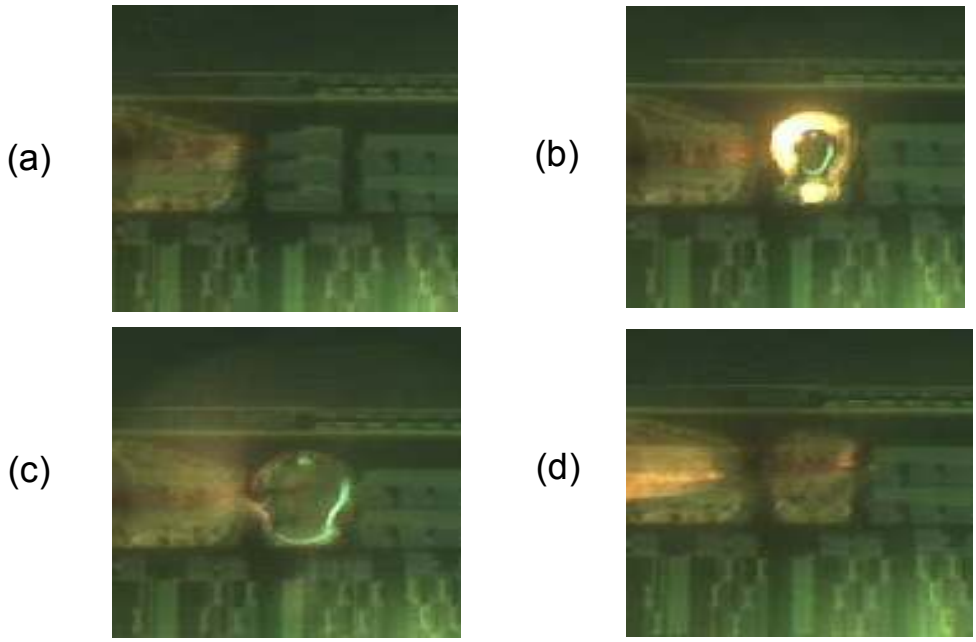


Fig. 5.3 In-situ video recording of the micro-injection on the devices; (a) the orange rod at the left side of picture is the tip of the micropipette. The micropipette is positioned by the manipulator for injection of the PDI-8CN_2 solution (b) semiconductor solution is injected to the devices (c) injected solution starts to dry and crystallize (d) micropipette moves to the next target

5.3 Experiments and discussion

5.3.1 N-CHANNEL FIELD-EFFECT TRANSISTORS

Optimization of the process parameters and surface treatment was performed for solution-deposited PDI-8CN_2 OFETs and solution-based complementary circuits. Annealing temperature, solution concentration, aliphatic chain length in the SAMs for the dielectric surface treatment, and the SAMs for the source/drain surface treatment were chosen as the optimization parameters. Solution-based PDI-8CN_2 OFETs were fabricated on bottom-gate, bottom-contact configurations. A heavily doped p-type Si substrate served as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric layer, leading to an estimated capacitance of 34.5 nF/cm^2 per unit area of the gate dielectric. The electrodes were patterned photolithographically with 2.5 nm of Ti and 35 nm of Au deposited as source and drain electrodes by e-beam evaporation. The channel width and length were 200 μm and 4 μm, respectively. After lifting off, all samples were cleaned in an ultrasonic bath using acetone and methanol for 2 min each, and then rinsed with deionized water. The samples were next cleaned with the oxygen plasma to remove organic contaminants on the surface and to make the dielectric layer more hydrophilic. During PDI-8CN_2 solution jetting, the substrates were maintained at 110 °C to prevent coalescence of the ejected droplets, and the films were subsequently annealed on a 110 °C hot plate for 20 min under nitrogen ambient.

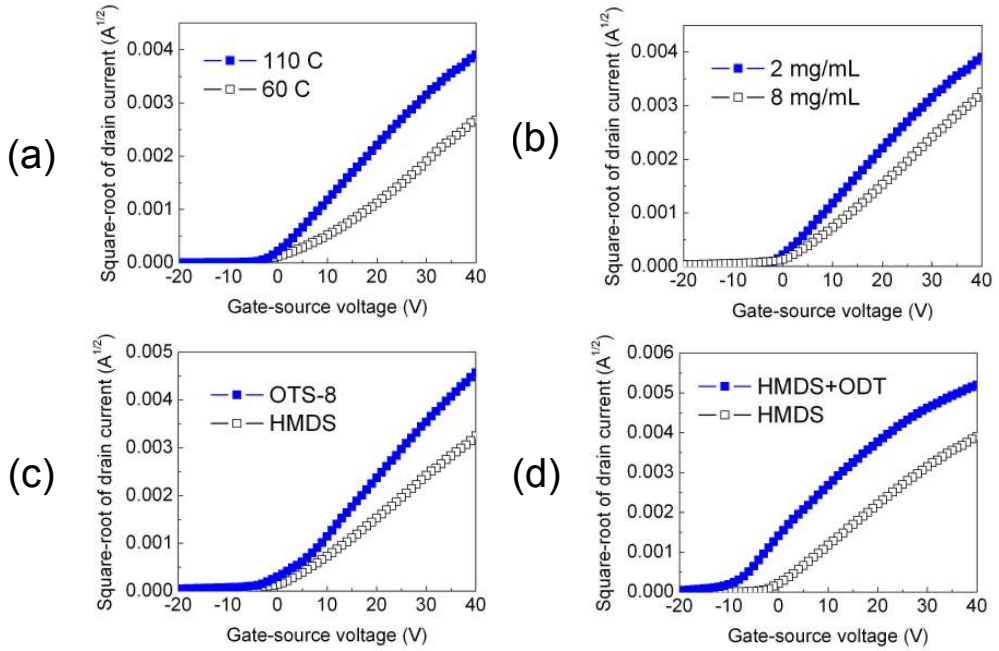


Fig. 5.4 Square-root of drain current versus gate voltage plots at V_{DS} = 40 V for OFET devices fabricated using varied process parameters and gate dielectric and/or electrode surface treatments. (W / L = 200 μm / 4 μm). a) Annealing temperature: 60 °C (open squares), 110 °C (filled squares). b) Solution concentration: 2 mg/mL (filled squares), 8 mg/mL (open squares). c) Gate dielectric treatment: hexamethyldisilazane (HMDS) (open squares), OTS-8 (filled squares). d) Source/drain electrode treatment: HMDS-treated (open squares), HMDS + ODT treated (filled squares)

Fig 5.4 shows the square-root of drain current versus gate voltage characteristics of devices fabricated with varied process parameters and surface treatments at a source-drain voltage of 40 V. The device structure and dimensions are held constant in all cases. Carrier mobility is the most crucial factor affecting circuit speeds and can be calculated from the slope of the square-root of drain current versus gate voltage plots in the saturation regime. Optimized results were obtained for devices fabricated at higher annealing

temperatures, lower solution concentrations, longer chain dielectric coating agents, and with electrode surface treatment using thiol-based SAMs. It is likely that higher annealing temperatures eliminate residual solvent, oxygen, and moisture from the film, and also favor the reconstruction of more ordered films. Dilute solutions prevent PDI-8CN_2 aggregation in solution prior to deposition and retard film growth, possibly enhancing reflow and recrystallization. Gate dielectric treatment experiments show that longer aliphatic chains of OTS-8 are more favorable than HMDS for ordered PDI-8CN_2 film deposition, probably reflecting a decrease in surface energy differences at the dielectric/semiconductor interface [39,131,132]. Thiol-based SAMs, such as ODT, have similarly been proved to enhance the performance of OFETs [42,43,90].

Consequently, optimized solution-deposited PDI-8CN_2 OFETs were fabricated and the output characteristics of bottom contact OFETs are shown in Fig 5.5. Prior to the deposition of the PDI-8CN_2 solutions, various surface treatments were performed. For the gate dielectric SAM, the samples were exposed to OTS-8 vapor under nitrogen. Metal electrode surface treatment was performed by immersing the samples in a 5mM solution of ODT in ethanol under nitrogen. The final fabrication step is jetting the PDI-8CN_2 solution. During the deposition process, substrates were heated and annealed on a hot plate for 20 min at 110 °C in nitrogen ambient. Channel width and length are 200 and 4 μm, respectively.

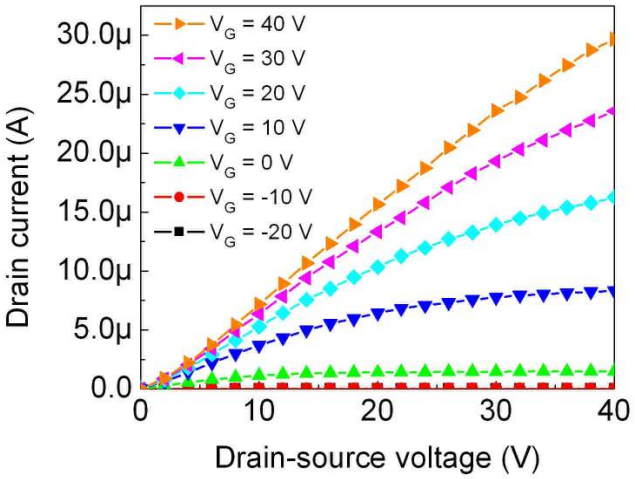


Fig. 5.5 Output characteristics of 4 μm channel length (W / L = 50) PDI-8CN_2 solution-processed bottom contact OFETs with OTS-8 + ODT surface treatments at V_D = 40 V, measured at ~10^{-3} Torr. A heavily doped p-type Si substrate serves as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric. The calculated saturation regime mobility and threshold voltage are 2.4 X 10^{-2} cm^2/Vs and -1.1 V, respectively

While operating under vacuum, the saturation regime mobility and threshold voltage were measured to be 2.4 X 10^{-2} cm2/Vs and -1.1 V, respectively. This mobility is about five times less than that of vapor-deposited PDI-8CN_2 films due to morphological/microstructural irregularities. However, it is the highest organic n-channel solution processed OFET mobility obtained so far for channel lengths lower than 10 μm [125,128]. Fig 5.6 shows the AFM images of a sublimed PDI-8CN_2 film and a solution-based PDI-8CN_2 film. The grain size of the solution-based PDI-8CN_2 film on SiO_2 was approximately 800 nm and the rms roughness was 5.8 nm. The AFM image of the solution-based PDI-8CN_2 film reveals a moderately rough morphology and a smaller grain size which

results in a large number of grain boundaries. The density of trap states is high in the grain boundaries, resulting in the degradation of solution-deposited OFETs.

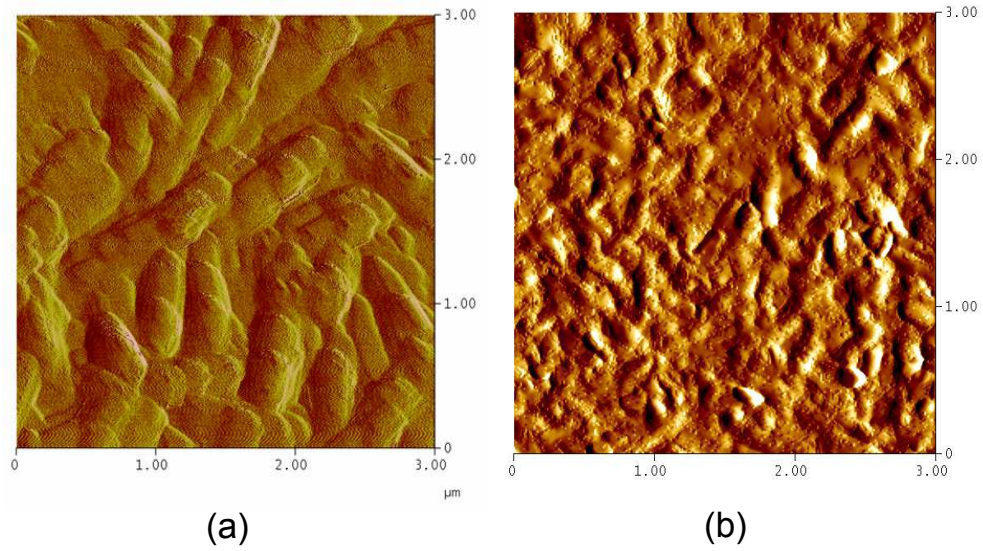


Fig. 5.6 The Atomic force microscopic images of (a) sublimed PDI-8CN_2 film and (b) solution-based PDI-8CN_2 film. The rms roughness of the solution-based film is 5.8 nm determined for a 3 μm X 3 μm AFM scan size with 256 points per line.

To assess the thin film microstructure, x-ray diffraction (XRD) experiments were performed with both vapor deposited and solution-processed PDI-8CN_2 films on HMDS-treated Si/SiO_2 substrates as shown Fig 5.7. Thin film XRD characterization was performed using a Rigaku ATXG thin film diffractometer with Ni-filtered Cu Kα radiation. The θ/2θ scans of both vapor- and solution-deposited films indicate a significantly textured thin film microstructure, where the molecular long axes are tilted at ~40^o with respect to the substrate plane. The peaks of sublimed PDI-8CN_2 film are relatively more

distinct due to better crystallinity. From the 00*l* reflections in the θ/2θ scans, a *d*-spacing of 19.7 ± 0.1 Å is calculated for both films.

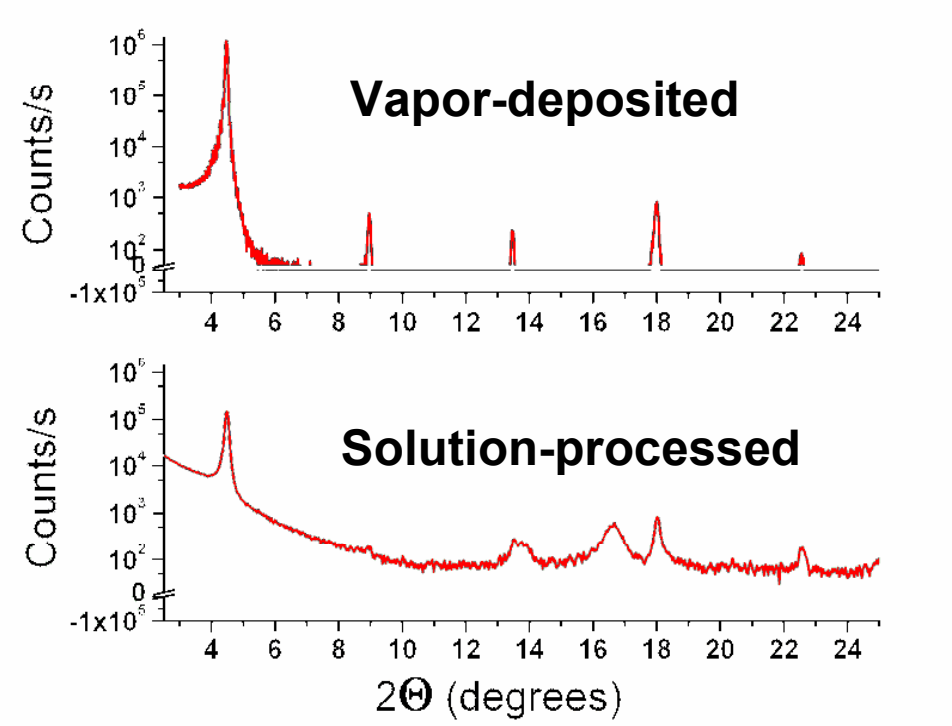


Fig. 5.7 X-ray diffraction patterns for (a) a vapor-deposited PDI-8CN_2 film on HMDS-treated SiO_2 and (b) a solution-processed PDI-8CN_2 film on HMDS-treated SiO_2, indicating high crystallinity for both films, and room for improved ordering in the solution-processed film

The *001* Bragg reflections for both vapor-deposited and solution-deposited PDI-8CN_2 films are shown in Fig 5.8. Fig 5.8(a) exhibits Laue oscillations, indicating a highly-ordered microstructure for sublimed films. The inset of Fig 5.8(a) shows a rocking curve (full-width-half-maximum, FWHM, = 0.03°), indicating small distributions of lattice plane orientations. In contrast to the sublimed film, Laue oscillations are not observed for the solution-deposited film,

and broadening of the rocking curve (FWHM = 0.07°) indicates a greater level of complexity as shown Fig 5.8(b). The XRD data suggest that further optimization of the solution deposition conditions is possible, which could lead to mobilities comparable to those observed for vapor-deposited films.

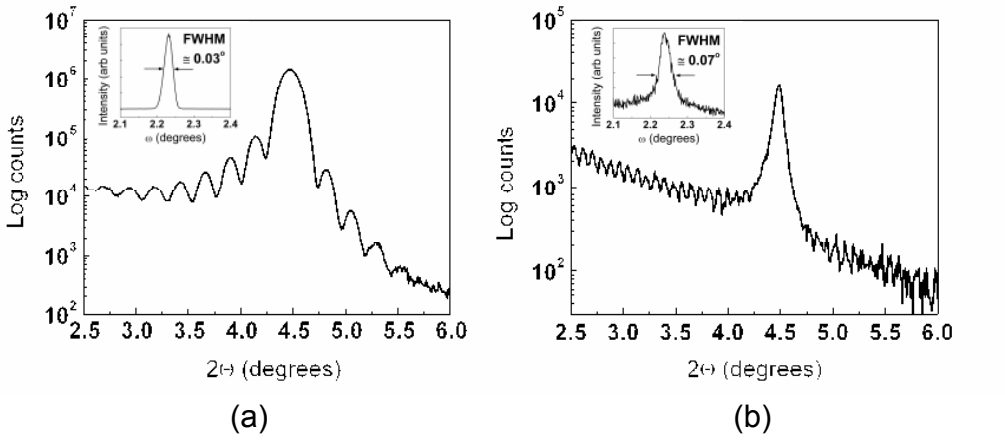


Fig. 5.8 Typical x-ray reflectivity scans of (a) a vapor-deposited PDI-8CN_2 film on HMDS-treated SiO_2 and (b) a solution-processed PDI-8CN_2 film on HMDS-treated SiO_2. The Sublimed PDI-8CN_2 film exhibits Laue oscillations indicating quality of layering. The insets show the rocking curves (full width half maximum (FWHM)) (a) 0.03° and (b) 0.07°

5.3.2 COMPLEMENTARY CIRCUITS

Utilizing these optimization results for PDI-8CN_2 solution deposited films, five-stage complementary ring oscillators and complementary pass transistor logic based D flip-flops were fabricated with PDI-8CN_2 solution-deposited n-channel FETs and poly(3-hexyl)thiophene (P3HT) solution-deposited p-channel FETs.

These complementary circuits, consisting of both p-channel and n-channel transistors, are an ideal configuration for organic semiconductors, offering low static power dissipation, crucial for the portable, often battery operated applications envisioned for organic-based electronics, and the superior noise margins which relax the requirement for large I_{on}/I_{off} ratios.

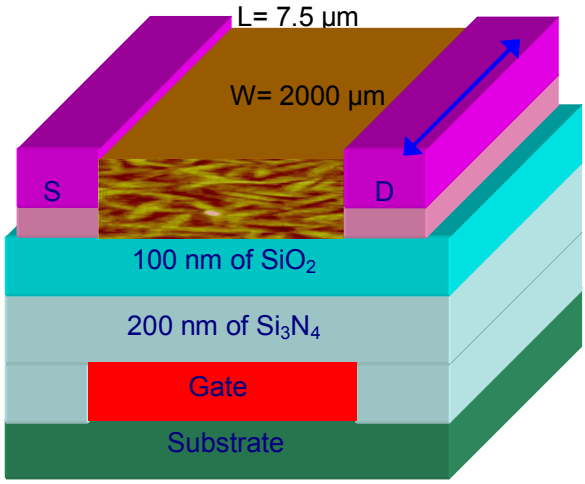


Fig. 5.9 Schematic of the organic transistor used in circuits. The gate dielectric consists of a bilayer which is 200 nm of silicon nitride and 100 nm of silicon dioxide. Channel length and width are 7.5 µm and 2000 µm, respectively.

The basic circuit fabrication details have been discussed previously [71]. The present solution-based CMOS devices were fabricated with both OTS-8 and ODT treatments, with the substrate temperature during film growth being 110 °C, and the annealing temperature being 110 °C for 20 min under nitrogen ambient after solution patterning. The channel width and channel length of the individual transistors were 2000 µm and 7.5 µm, respectively. Solutions of PDI-8CN_2 and P3HT were employed in concentrations of 2 mg/mL and 10 mg/mL, respectively,

under a nitrogen ambient. All solutions were filtered through a 0.2 μm size PTFE syringe filter before use. The structure of discrete OFETs is the same as mentioned in chapter 4 and illustrated in Fig. 5.9. Electrical characterization was conducted in vacuum and air at room temperature with an Agilent 4155C semiconductor parameter analyzer. Fig 5.10 shows the output characteristics of the discrete OFETs measured in both vacuum and air. The saturation region mobility of PDI-8CN$_2$ films is reduced slightly from 1.4×10^{-2} cm^2/Vs to 8.9×10^{-3} cm^2/Vs after exposure to air. The saturation region mobilities of P3HT in vacuum and air are 2.6×10^{-2} cm^2/Vs and 2.4×10^{-2} cm^2/Vs, respectively.

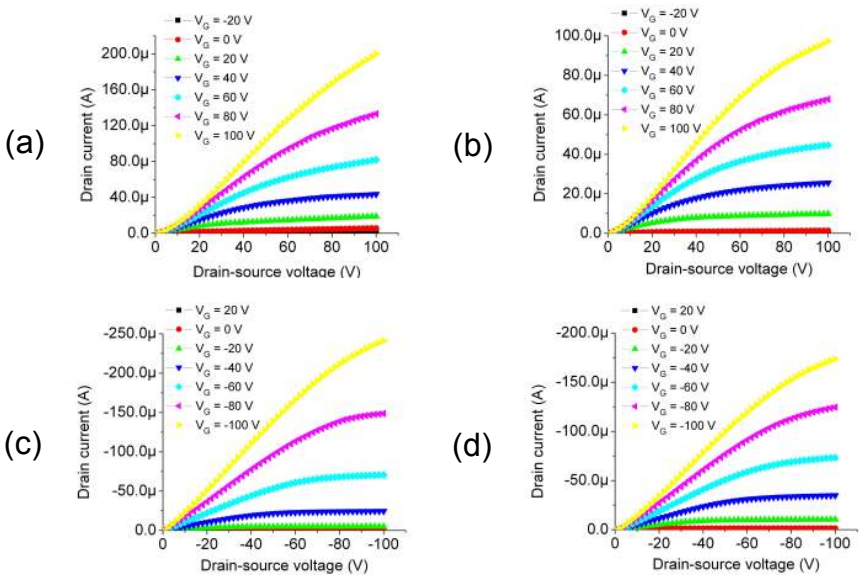


Fig. 5.10 (a) output characteristics of a PDI-8CN$_2$ transistor in vaccum. The saturation regime mobility is 1.4×10^{-2} cm^2/Vs (b) output characteristics of PDI-8CN$_2$ transistor in air. The saturation regime mobility is 8.9×10^{-3} cm^2/Vs (c) output characteristics of P3HT transistor in vaccum. The saturation regime mobility is 2.6×10^{-2} cm^2/Vs (d) output characteristics of P3HT transistor in air. The saturation regime mobility is 2.4×10^{-2} cm^2/Vs. The gate dielectric consists of a bilayer which is 100 nm of silicon dioxide on 200 nm of silicon nitride. Channel length and width are 7.5 μm and 2000 μm, respectively

A ring oscillator, often used in clock generation circuits, was fabricated by connecting an odd number of inverters in a loop. A LeCroy 6030 oscilloscope was used to evaluate the output characteristics of the ring oscillators and D flip-flops. The measurement setups for testing ring oscillators and D flip-flops are the same as those described in the previous chapter. Fig 5.11 shows the output characteristics of a five-stage ring oscillator using P3HT and PDI-8CN_2 solution with a supply voltage of 100 V and a channel length of 7.5 μm. Oscillation frequencies of 3.2 kHz and 2.2 kHz are achieved in vacuum and in ambient atmosphere at room temperature, respectively. In comparison with the results using sublimed semiconductor layers, the maximum oscillation frequency is lower by approximately one order of magnitude due to lower mobility of each solution-deposited transistor.

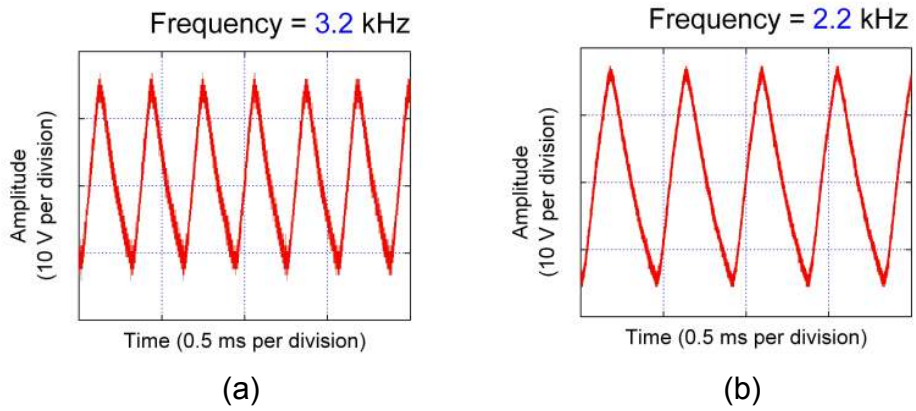
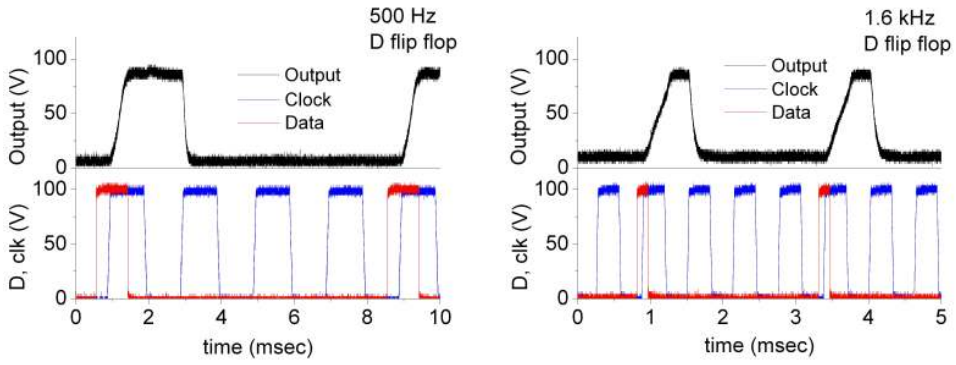


Fig. 5.11 Output characteristics of a five-stage complementary ring oscillator. PDI-8CN_2 solutions and poly(3-hexyl)thiophene (P3HT) solutions were used for n-channel FETs and p-channel FETs, respectively. The supply voltage is 100 V. (W / L = 2,000 μm / 7.5 μm). (a) oscillation frequency of 3.2 kHz in vacuum (b) oscillation frequency of 2.2 kHz in air

The edge triggered D flip-flops are a critical component of sequential logic circuits and usually composed of two level sensitive latches. The electrical characterization of the D flip flops was carried out in ambient atmosphere at room temperature. The measured characteristics for the pass transistor logic-based D flip-flop at clock frequencies of 500 Hz and 1.6 kHz at a supply voltage of 100 V are shown in Fig 5.12(a) and (b), respectively. The measured output, clock signal, and data signal are represented by a black line, a blue line, and a red line, respectively. The output begins to degrade at 1.6 kHz. However, it is still controlled by the clock signal. These results represent the first organic complementary circuits based solely on solution-deposited active semiconductors, and represent a major step forward in developing printed organic electronic circuits with high switching speeds, low noise margins, and low power dissipation.



(a) (b)

Fig. 5.12 Output characteristics of complementary D flip flops. The supply voltage is 100 V. (W / L = 2,000 μm / 7.5 μm). The black line, blue line, and red line represent the measured output, clock signal, and data signal, respectively. All measurements are carried out in air. Operation at (a) 500 Hz and (b) 1.6 kHz

5.4 Conclusion

We have demonstrated that PDI-8CN_2 is not only a promising n-channel semiconductor deposited by sublimation, but also a promising semiconductor for solution-processed n-channel OFETs. Various parameters such as the annealing temperature, solution concentration, aliphatic chain length in the SAMs for the dielectric surface treatment, and the SAMs for the source/drain surface treatment are compared for the optimization of the process for fabricating high performance devices. A saturation regime mobility of 2.4×10^{-2} cm^2/Vs and threshold voltage of -1.1 V are obtained at V_{DS} = 40 V with both OTS-8 and ODT treatments. The XRD results suggest that further optimization of the solution deposition conditions leads to the achievement of a comparable quality of semiconductor films prepared using vacuum deposition techniques.

Utilizing optimized process parameters and surface treatments for solution-deposited PDI-8CN_2 OFETs, we have shown for the first time, the fabrication of complementary organic circuits in which both p- and n-channel materials are solution deposited, yielding complementary ring oscillators and D-flip flops that operate in air without passivation or packaging. The ring oscillator operating frequencies are in the range of 2-3 kHz for 7.5 μm channel length devices, and the flip-flops operate with clock frequencies in excess of 1 kHz. Performance of the devices can be improved by increasing the n-channel mobility further as well as by reducing channel lengths and overlap capacitances between the source/drain electrodes and the gate. The enabling advancement in this context is the successful development of an air-stable n-type organic

semiconductor, PDI-8CN_2, along with compatible solution deposition processing techniques.

CHAPTER 6 NANOWIRE TRANSISTORS

6.1 Introduction

With organic semiconductors, one-dimensional nanostructures such as semiconductor nanowires and carbon nanotubes have attracted much attention for future electronic applications such as FETs, light-emitting diodes, memory elements, and chemical sensors [50-52,133]. Germanium (Ge) nanowires have recently gained interest as potential FET channel materials due to their higher carrier mobilities than silicon, solution processibility, and their potentials for low cost mass production and integration with organic electronic materials on flexible substrates. However, the transport properties of Ge nanowires are sensitive to the surface chemistry, with hysteresis in gate potential scans along with time-dependent decay in gate response due to the presence of slow surface states [134].

In this chapter, we demonstrate the characteristics of the bottom-contact devices with Ge nanowires as a semiconducting layer on the Ti/Au electrodes. Ge nanowires are not intentionally doped during or after the synthesis and passivated with an organic monolayer, isoprene. The use of EG-treated PEDOT electrodes was discussed in chapter 3. We combined this technique to the fabrication of top-contact FET with organic monolayer passivated Ge nanowires. Their electrical properties will be also reported.

6.2 The synthesis of germanium nanowires

The germanium nanowires were synthesized and supported by Prof. Korgel at the University of Texas at Austin. The supercritical fluid-liquid-solid (SFLS) method was approached in a continuously-stirred 250 mL PARR reactor [134-136]. This reaction yields approximately 1 g of crystalline Ge nanowires in a single reaction. Anhydrous hexane with 34.8 mM diphenylgermane (DPG, Gelest) and 3 nm diameter dodecanethiol-coated Au nanocrystals were continuously fed into the reactor at a Au:Ge mole ratio of 1:1200 at 380^{o}C and 800 psi at a flow rate of 7 mL/min [137]. The average residence time in the reactor is 35 min and the total volume of hexane, DPG, and Au nanocrystals used were 500 mL, 3.25 mL and 1.25 mL, respectively. Before removing the nanowires from the reactor, they were passivated with an organic monolayer by hydrogermylation of the Ge surface with isoprene. This organic monolayer coating has been shown to significantly improve carrier mobility and prevent surface oxidation [138]. To coat the nanowires, the reactor was cooled to 250^{o}C and the pressure increased to 1100 psi by adding more hexane. 25 mL of isoprene was added, which increased the pressure to 2300 psi. The reactor was then cooled to 145^{o}C, flushed with hexane at 5 mL/min for 25 min, and then further cooled to 75^{o}C and flushed again with hexane at 5 mL/min for 10 min. The reactor was cooled to room temperature and the wires were removed from the reactor. The Ge nanowires predominantly align to a <110> growth direction.

6.3 Bottom-contact transistors

The bottom-contact Ge nanowire FETs are fabricated using micro-injection of the nanowire solution as shown in Fig. 6.1. The substrate is a heavily doped n-type silicon substrate as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric layer. The capacitance of gate dielectric was appoximately 35 nF/cm^2. 2.5 nm of Ti adhesion layer and 35 nm of Au layer were patterned by photolithography and e-beam evaporation. Channel length of device was 4 μm. To remove residual organic contaminants on the surface, the substrates were oxygen plasma cleaned (50 W) for 1 min. Prior to the injection of Ge nanowire solution, HMDS treatment was used to make the gate dielectric hydrophobic. HMDS treatment was performed by exposing the freshly cleaned substrates to HMDS vapor for 20 hr under nitrogen. The sonication of nanowire solution is critical for preventing the entanglement of nanowires in the solution. Fig. 6.2 shows the example which is the scanning electron microscope (SEM) image of entangled zinc selenide nanowires on the patterned devices without the sonication. Therefore, the Ge nanowire solutions were sonicated for 5 min before use. The injection of Ge nanowire solution was performed by Picospritzer® system in air as described in the previous chapter. The concentration of Ge nanowire solution was 0.2 mg/mL. All electrical characterizations were carried out in vacuum (~1 mTorr) at room temperature with an Agilent 4155C semiconductor parameter analyzer.

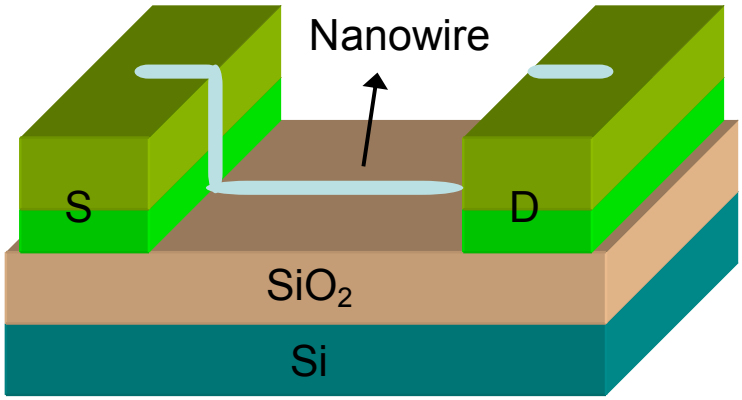


Fig. 6.1 Schematic representation of Ge nanowire bottom contact transistors. A heavily doped p-type silicon substrate served as the gate electrode with 100 nm of thermally grown SiO_2 layer as the dielectric. 2.5 nm of Ti and 35 nm of Au were evaporated as source/drain electrodes. The concentration of Ge nanowire solution was 0.2 mg/mL and it is deposited using micro-injection technique

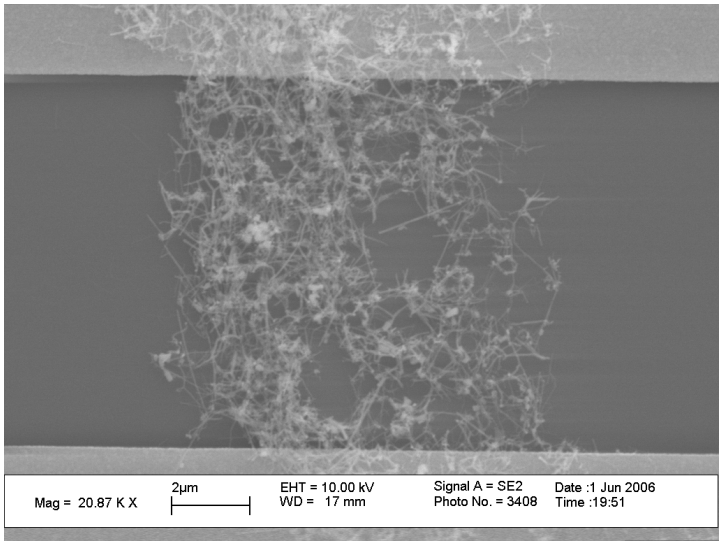


Fig. 6.2 The scanning electron microscope (SEM) image of entangled zinc selenide nanowires on the 12 µm channel length devices

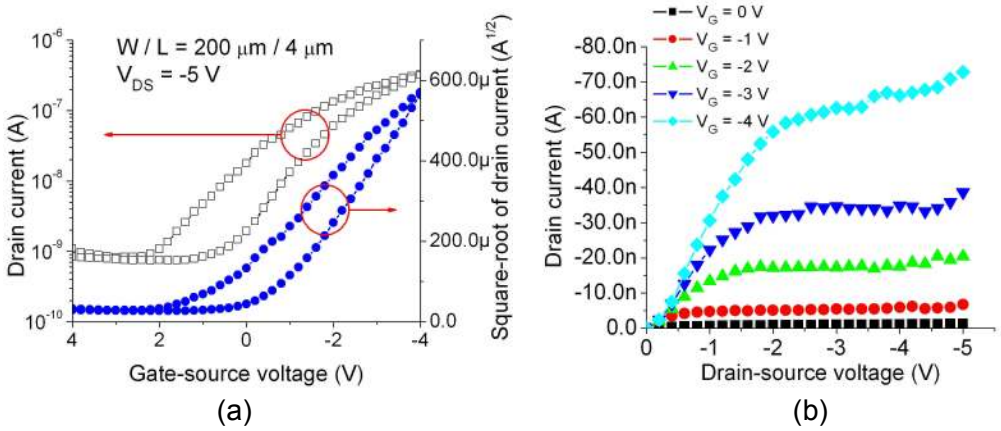


Fig. 6.3 (a) transfer and (b) output characteristics of 4 μm channel length bottom-contact FETs with Ge nanowires as the channel layer

The transfer and output characteristics of 4 μm channel length bottom-contact Ge nanowire FETs are represented in Fig. 6.3. It is well known that Ge tends to accumulate holes at the semiconductor surfaces and acts as a p-type semiconductor [138,139]. The output characteristic shows the saturation regime at the high drain voltage region. Low off-current was also obtained in the bottom-contact Ge nanowire FETs. However, the drain current is not enough high and the hysteresis was found in the transfer characteristic possibly due to the residues of organic solvent. Fig. 6.4 presents the SEM images of this bottom-contact Ge nanowire FETs. It is shown that two Ge nanowires are connected between source and drain electrodes. The insets show the magnification of boundary between Ge nanowires and the electrodes. The Ge nanowires range from 10 nm to 70 nm in diameter.

However, the fabrication yield of bottom-contact Ge nanowire FETs was very low as of approximately 2 % with simple injection technique because the

alignments of nanowires were done by chance. Accordingly, the other approaches to get better performance of nanowire transistors are concerned as well as the reproducibility in next section.

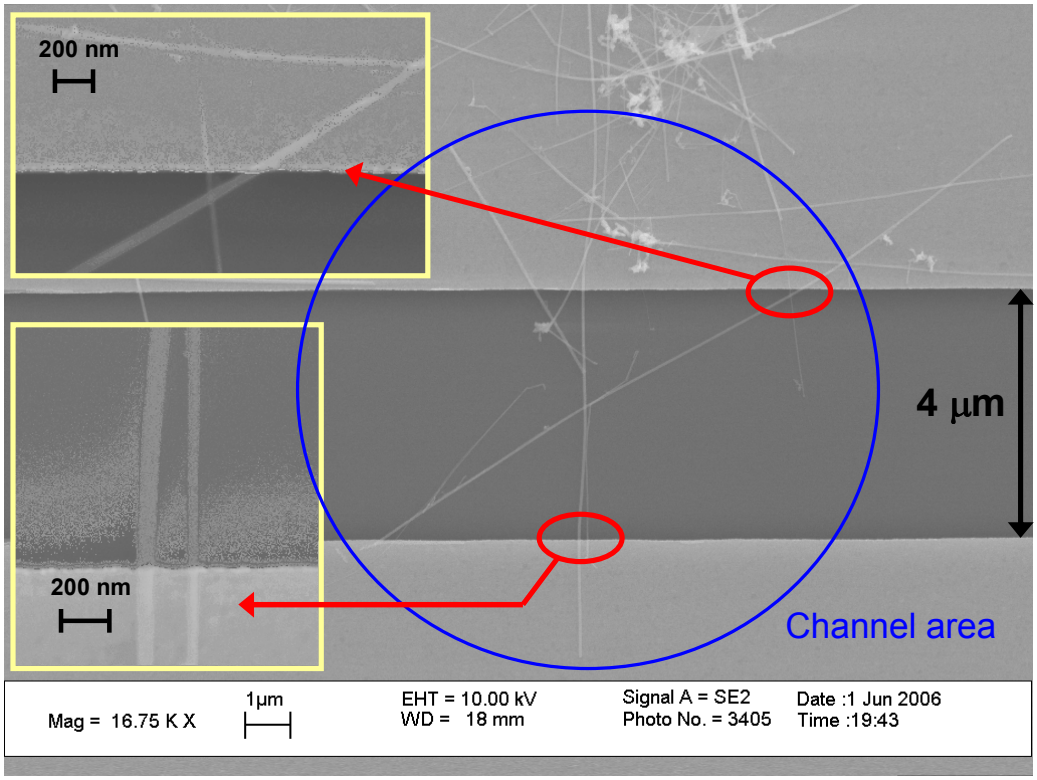


Fig. 6.4 The SEM images of 4 μm channel length (W / L = 50) bottom-contact FETs. Two Ge nanowires are connected between source and drain electrodes. The insets show the magnification of boundary between Ge nanowires and the electrodes

6.4 Top-contact transistors with PEDOT/PSS electrodes

One of major issues in device fabrication is the development of reliable electrical contacts between nanowires and electrodes [140]. Another challenge is fabrication of flexible electronic devices: to achieve this goal, the device components, such as the electrodes and semiconductors, should be solution-processable. Although several studies have shown an improvement of electrical contacts using the passivation of nanowires and various fabrication techniques such as focused ion beam and focused electron beam [140,141], the use of a polymer electrode, which has better contact properties with the organic passivation layer has not yet been reported. The biggest obstacle to using solution-processable organic electrodes has been their very low conductivities compared with evaporated metal electrodes. We exploited the modifications of conducting polymer to fabrication of OFETs in chapter 3 and applied this improvement to the fabrication of Ge nanowire FETs again.

Fig. 6.5 outlines the fabrication process for Ge nanowire FETs with PEDOT electrodes. The substrate is n-doped silicon, which serves as the gate electrode with 100 nm of thermally grown SiO_2 as the dielectric layer. All substrates were sonicated in acetone and methanol for 2 min and rinsed with deionized water. Ge nanowires were suspended in ethanol, and then deposited onto the substrate by drop-casting [Fig. 6.5(a)]. HMDS vapor was exposed to the substrate and photoresist (PR) was patterned by photolithography with channel lengths of 4 and 12 μm [Fig. 6.5(b)]. The substrates were then oxygen plasma treated (50 W) for 30 sec to make the dielectric layer hydrophilic and a

PEDOT/PSS aqueous solution was directly spun cast on the treated substrates. The PEDOT/PSS film was dried at 90 °C for 15 min on the hot plate. The substrate was then immersed in the EG for 3 min to enhance the conductivity of the PEDOT/PSS film and subsequently dried at 90 °C for 10 min [Fig. 6.5(c)]. After lift-off, all samples were carefully cleaned in acetone and methanol [Fig. 6.5(d)]. The samples were then annealed at 200 °C for 30 min under a nitrogen environment. The nanowires were characterized by high resolution scanning electron microscopy (HRSEM, LEO1530) and all electrical characterizations were carried out under vacuum (~1 mTorr) at room temperature with an Agilent 4155C semiconductor parameter analyzer.

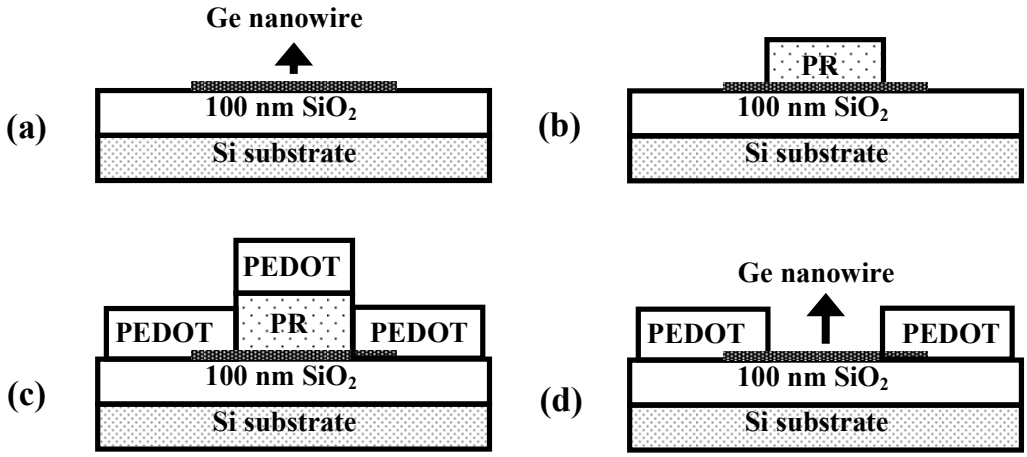
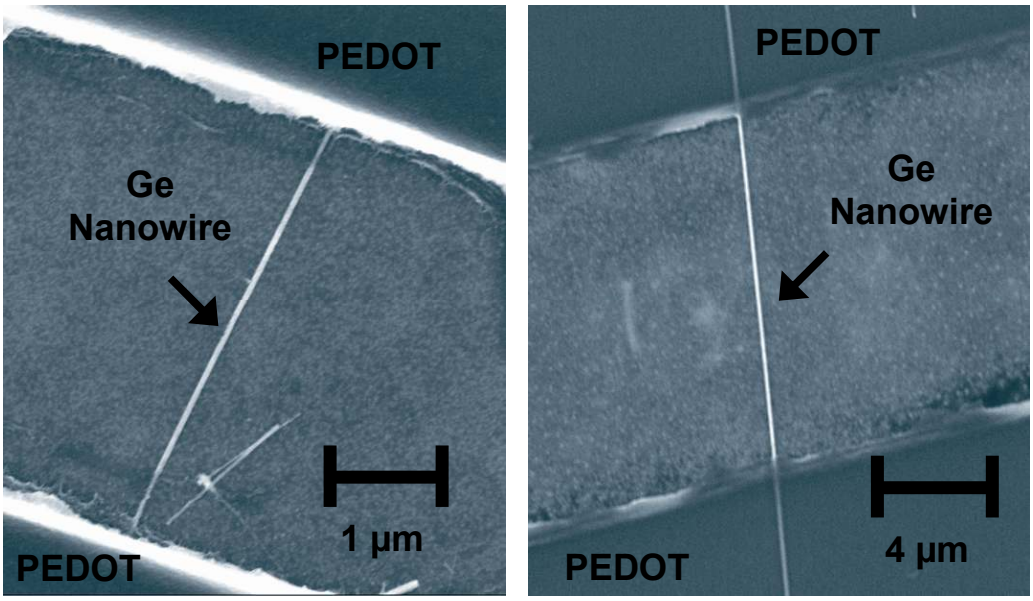


Fig. 6.5 The process step of Ge nanowire bottom contact device using PEDOT/PSS electrodes with 100 nm of thermally grown SiO_2 layer as the gate dielectric. (a) drop cast Ge nanowires onto the substrate. (b) photolithographically patterned photoresist. (c) spin coat the PEDOT/PSS aqueous solution, and ethylene glycol treatment. (d) lift-off the photoresist. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 90, 072106 (2007). Copyright 2007, American Institute of Physics

Fig. 6.6 shows scanning electron microscopy (SEM) images of Ge nanowire devices contacted by EG-treated PEDOT electrodes on SiO_2 dielectric layer. The measured diameter of the nanowire is approximately 40 nm. The channel lengths are 4 μm [Fig. 6.6(a)] and 12 μm [Fig. 6.6(b)], respectively. SEM images confirm that only one Ge nanowire was connected between electrodes for each FET while the density of nanowires on the substrate could be controlled by varying the concentration of the nanowires in the solution.



(a) (b)

Fig. 6.6 SEM top-view images of Ge nanowire devices contacted with EG-treated PEDOT electrodes on SiO_2 dielectric layer. The diameter of nanowire is approximately 40 nm. The channel lengths are (a) 4 μm and (b) 12 μm, respectively. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 90, 072106 (2007). Copyright 2007, American Institute of Physics

The output characteristics of Ge nanowire transistor with EG-treated PEDOT electrodes are shown in Fig. 6.7. Out of 40 devices fabricated, 7 devices showed proper p-channel FET characteristics (yield = 17.5 %). The capacitance is calculated by the cylinder-on-plate model [142],

$$C_{OX} = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\{(b+h)/b\}} = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln[\{(b+h)/b\} + \sqrt{\{(b+h)/b\}^2 - 1}]}$$

where L is the channel length, b is the radius of nanowire, h is the thickness of SiO_2 dielectric layer, and ε_r is the dielectric constant of the SiO_2 dielelctric (ε_r = 3.9). For b = 20 nm and h = 100 nm, the capacitance of 4 μm channel length Ge nanowire device is 0.35 fF. The mobility can be calculated by the linear region transconductance [143],

$$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L^2}{V_{ds} C_{ox}}$$

The estimated carrier mobility for the 4 μm channel length device is 0.3 cm^2/Vs in Fig. 6.7(a) and the mobility was observed to significantly vary from sample to sample. For example, the calculated carrier mobility for 12 μm channel length device is 7.0 cm^2/Vs in Fig. 6.7(b) and this device shows higher mobility than the device using focused ion beam assisted Pt electrodes [136,138]. However, this mobility value is still several orders of magnitude lower than ideal mobility in bulk Ge. The cylinder-on-plate model is based on the assumption that the nanowire is embedded in the dielectric. However, the nanowire is deposited on top of the gate dielectric. It is expected that gate capacitance is reduced by a factor of ~ 2 when h/b=5 [144]. Surface states on the nanowire also give rise to the weaker gate coupling and make the series capacitance which results in lower total capacitance. A more accurate expression of nonideal cylindrical nanowire capacitance is reported by Krčmar *et al.* [145]. In the

literature, the empirical effective dielectric constant of SiO2 were reported as $\varepsilon_{r,eff}$ = 1.95, 2.2, or 2.5 [144,146,147]. Therefore, the calculated mobility represented lower bound and the actual mobility would be higher due to the lower total capacitance.

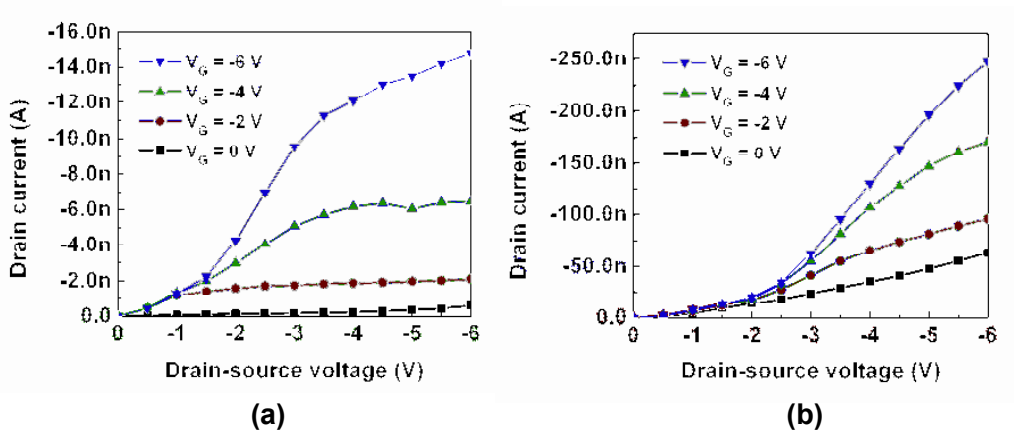


Fig. 6.7 Output characteristics of (a) 4 μm and (b) 12 μm channel length Ge nanowire FETs with EG-treated PEDOT electrodes under a vacuum atmosphere (~1 mTorr) at room temperature. The gate voltage was stepped in -2 V increments from 0 to -6 V. Reprinted with permission from Byungwook Yoo, *et. al.*, Appl. Phys. Lett. 90, 072106 (2007). Copyright 2007, American Institute of Physics

6.5 Conclusion

The bottom-contact Ge nanowires FETs with 4 μm channel length are fabricated and characterized as one of the promising alternatives for low cost fabrication on flexible substrates. Micro-injection technique was used to deposit the nanowire solutions. Devices showed the reasonable transistor operations which are low off-current and saturated drain current at the high drain voltage region. However, the fabrication yield of bottom-contact Ge nanowire FETs was low due to the spontaneous alignment of nanowires.

We have demonstrated that top contact Ge nanowire field-effect transistors can be fabricated with ethylene glycol treated PEDOT/PSS electrodes and exhibit reasonable device performance. Unlike Pt-contacted Ge nanowire FETs fabricated with the same isoprene-treated Ge nanowires grown by SFLS that had poor device performance and behaved like a gated resistor, these PEDOT/PSS contacted FETs show current saturation and reasonable on/off ratios, although the carrier mobility is still relatively low. The field-effect mobility was estimated to be 7.0 cm^2/Vs for a 12 μm channel length Ge nanowire FET, which appears to be limited by the nanowire itself and not the contacts. The use of solution processable nanowires and electrodes may enable the low cost production of flexible nanowire transistor based circuits and systems.

CHAPTER 7 CONCLUSION AND PERSPECTIVES

Organic field-effect transistors with promising n-type semiconductors, DFHCO-4T and PDI-8CN_2, were fabricated and characterized. For the top-contact DFHCO-4T OFETs, the estimated saturation mobility, the threshold voltage, subthreshold swing, and I_{on}/I_{off} ratio (V_{DS} = 30 V) were 0.33 cm^2/Vs, 16.6 V, 2.5 V/decade and ~ 1 X 10^5, respectively. The floating electrode method was applied to determine the contact resistance in the top-contact OFETs. It is shown that the contact resistance is not a major problem for large size devices of top-contact configuration. The effect of dielectric/electrode surface treatment on the response of bottom-contact devices was also examined. With the utilization of both the gate dielectric and electrodes surface treatment, the saturation mobility, threshold voltage, sub-threshold swing, and Ion/Ioff ratio (V_{DS} = 40 V, V_G = -10 ~ 40 V) of bottom-contact PDI-8CN_2 OFETs were 0.14 cm^2/Vs, 1.6 V, 2.0 V/decade, and 5.7x10^4, respectively. The use of lower work function metal and alkanethiol surface treatment enabled to get improved performance of n-channel OFETs.

We investigated the new technique which is direct coating of PEDOT/PSS solution on the metal electrodes using the hydrophilic properties of PEDOT/PSS solution, and the contact resistance was also reduced by almost 100-fold in comparison with the devices used Au electrodes. The conductivity modification effect in PEDOT/PSS was employed to the fabrication of the OFETs. The device performance and the fabrication yield were improved with the small dimension

devices and it is caused by the stronger interchain interaction in the ethylene glycol treated PEDOT.

Organic complementary ring oscillators and D flip-flops were demonstrated with pentacene and PDI-8CN_2 as the p-type and n-type material, respectively. An oscillation frequency of 34 kHz was obtained at V_{DD} = 100 V with a five-stage ring oscillator. An organic complementary D flip-flop was operated up to 5 kHz of a clock rate of in air, which is the highest speed that any organic transistor-based complementary clocked circuit has achieved to date. The speed of these complementary circuits will be enhanced by increasing the mobility of n-channel further as well as reducing channel lengths and overlap capacitances between the source/drain electrodes and the gate.

PDI-8CN_2 was used for solution-processed n-channel OFETs and the various parameters are compared for the optimization of devices. Optimized results were obtained for devices fabricated at higher annealing temperatures, lower solution concentrations, longer chain dielectric coating agents, and with electrodes surface treatment using thiol-based SAMs. Utilizing optimized process parameters and surface treatments for solution-deposited PDI-8CN_2 OFETs, we have shown the first fabrication of complementary organic circuits in which both p- and n-channel materials are solution deposited, yielding complementary ring oscillators and D-flip flops that operate in air without passivation or packaging. The ring oscillator operating frequencies are in the range 2-3 kHz for 7.5 μm channel length devices, and the flip-flops operate with clock frequencies in excess of 1 kHz. The enabling advance is the successful development of an air-stable n-type organic semiconductor, PDI-8CN_2, along with compatible solution deposition processing techniques.

The Ge nanowires FETs were fabricated and characterized for a potential of integration with organic electronic materials. The devices exhibit reasonable device performance. The field-effect mobility was estimated to be 7.0 cm^2/Vs for a 12 μm channel length Ge NW FET, which appears to be limited by the nanowire itself and not the contacts. The ethylene glycol treatment was used to increase the conductivity of PEDOT/PSS electrodes in this device. The use of solution processable nanowires and electrodes may enable the low cost production of flexible nanowire transistor based circuits and systems.

These electronic devices have been enormously explored for the different applications due to the unique properties and the significant potential for inexpensive fabrication. Even though there are still many challenges and limitations in this field, it is anticipated that the developments of both materials and processing techniques will lead the realization of commercial applications.

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Vita

Byungwook Yoo was born in Seoul, Korea on February 18th 1975, the son of Myung Shik Yoo and Soon Hee Kim. He graduated from Senior High School Attached to College of Education, Dankook University in Seoul. He received the B.S. degree in ceramic engineering from Yonsei University, Korea in 2000 and served in the military from February, 1996 to April, 1998. He was employed as a research scientist at the Korea Institute of Science and Technology from January, 2001 to May, 2001. He entered the University of Texas at Austin in August, 2001 and earned the M.S. degree in Materials Science and Engineering from the University of Texas, Austin in 2003. He continued his study for Doctor of Philosophy in the Department of Electrical and Computer Engineering at the Microelectronics Research Center, the University of Texas at Austin. During the summer of 2004, he worked at the Samsung SDI as an intern researcher.

Permanent address: 113-1201 LG 1st Village, Sungbok Dong, Sooji-gu,
Yongin, Gyeonggi-do, Republic of Korea 448-980

This dissertation was typed by the author.